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VOICE OF THE ENGINEER

JULY 5
Issue 14/2007
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NETWORKING MOVES TO HOME AUTOMATION

Page 40

POWER WITH NO STRINGS ATTACHED

Page 31

RUNNING AN FPGA AT ASIC SPEED

Page 53

LOW-POWER TRANSCEIVERS

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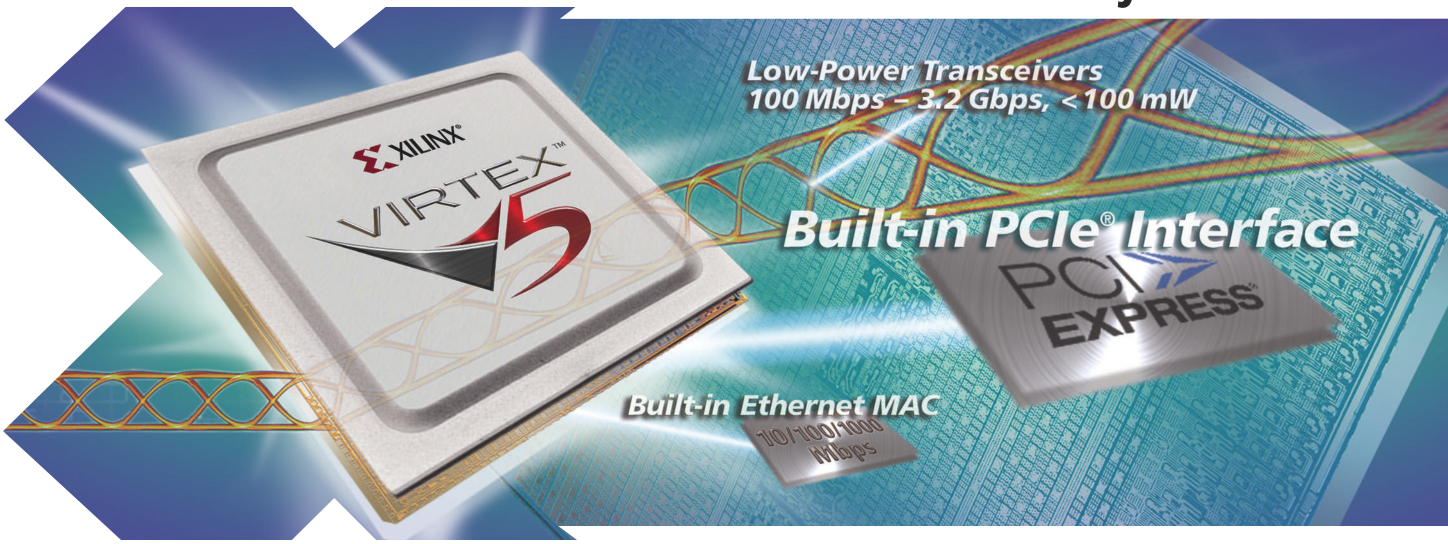

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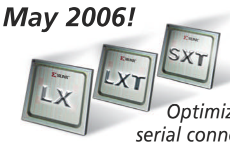

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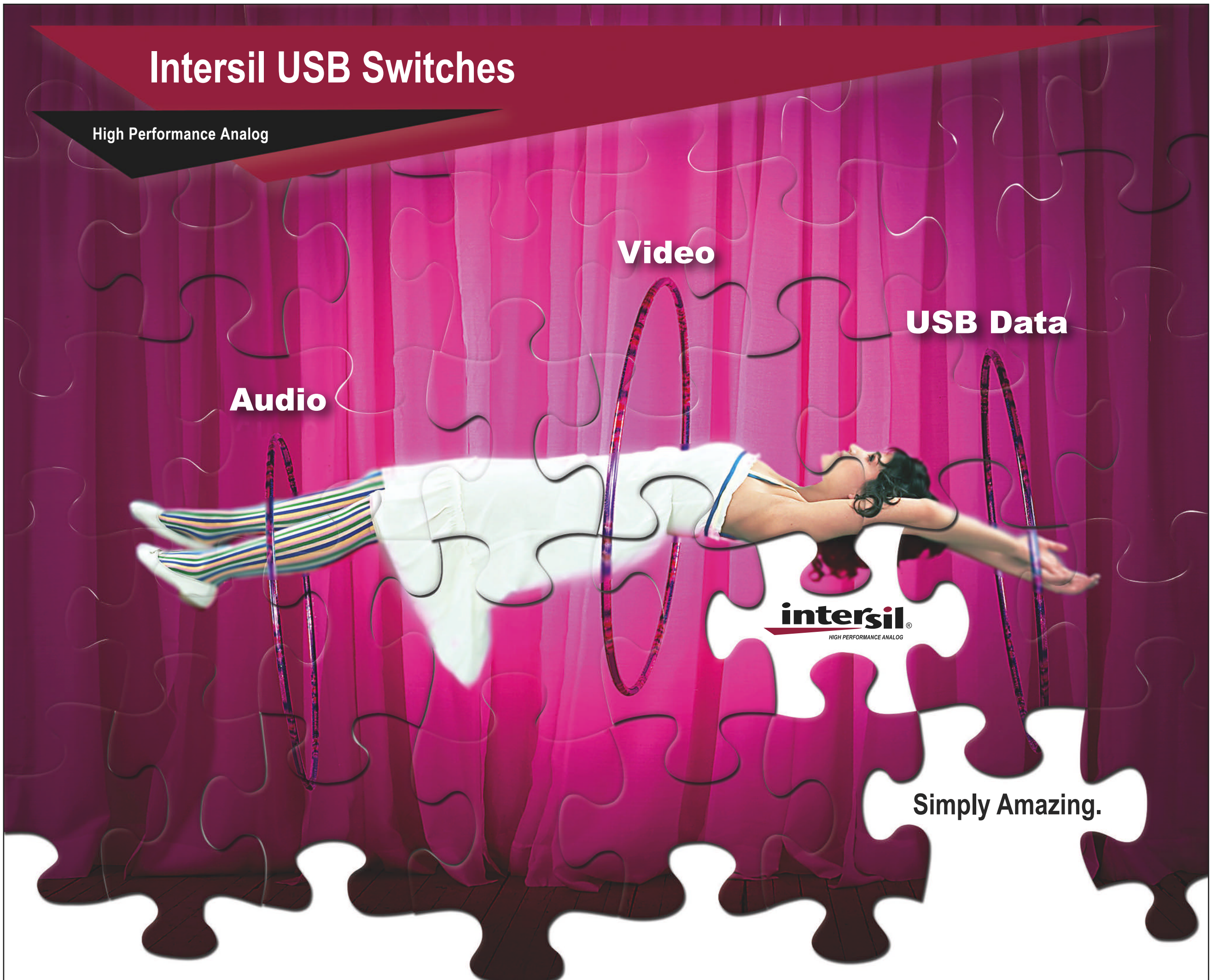

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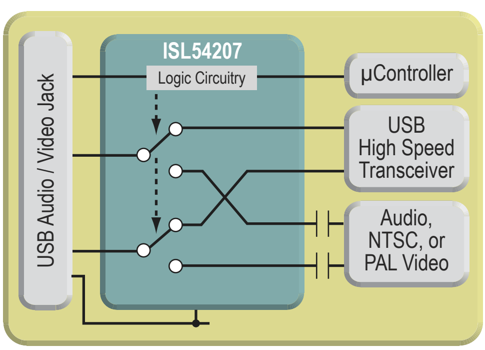
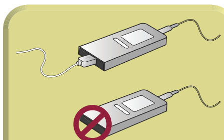
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03





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ISL54206	0.06	480
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ISL54401	0.007	12
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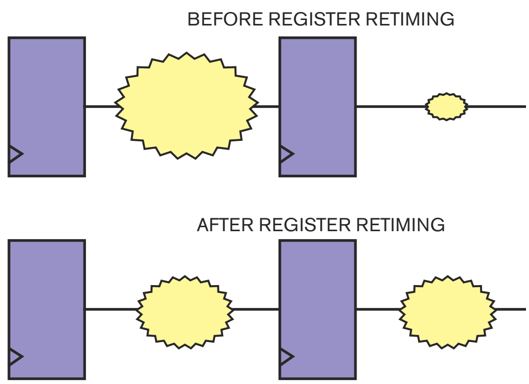
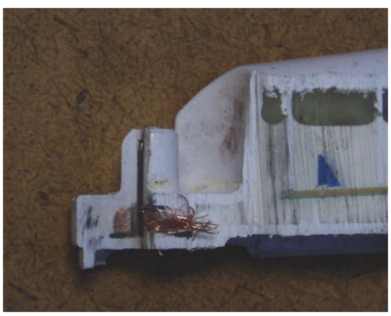


Networking moves to home automation



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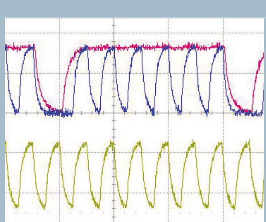

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contents 7.05.07

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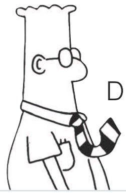
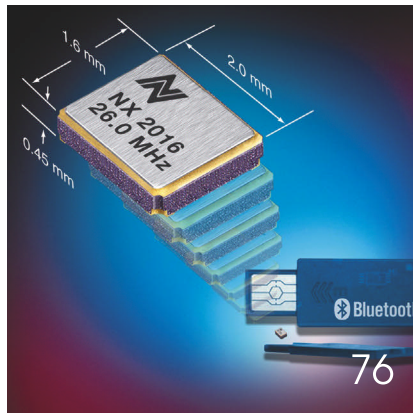


19

26



76

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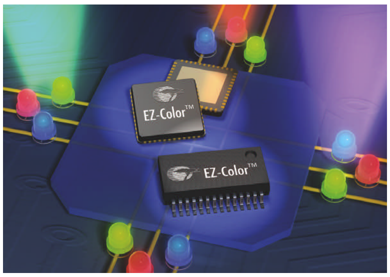

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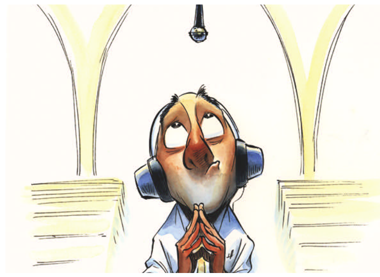

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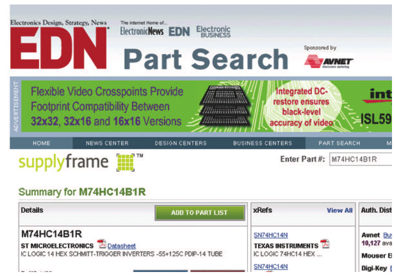

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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Homes still search for HD-capable video network

I have obsessed over the need for a relatively low-cost-networking technology that can carry HDTV streams around a home. I continue to believe that the video-networking application will drive big dollars for everyone from IC vendors to service providers and content owners. I've alternately been optimistic and skeptical over the prospects that IEEE 802.11 wireless technology could serve up whole-home video. More likely, most homes may have some wired backbones that connect wireless islands. I've also been optimistic and skeptical over how UWB (ultrawideband) might play in the video equation. Now, UWB proponents are getting serious about running their protocol over wire as well as the air.

In all fairness,a UWB over wires of various types isn't a new concept. Pulse-Link (www.pulselink.net) several years ago first pitched its CWave technology's ability to run over wires. The company then claimed that the same chip set could drive links over the air, power lines, phone lines, or coaxial cable. Pulse-Link is still pursuing the technology and has made subsequent IC announcements but doesn't appear to be shipping ICs for revenue.

Lately, some of the more mainstream WiMedia (www.wimedia.org) UWB crowd is touting that technology as a candidate for distributing digital video over coax. At the National Association of Broadcasters show (www.nabshow.com) in Las Vegas in April, Sigma Designs (www.sigmadesigns.com) demonstrated video over a UWB link. Sigma has focused on set-top boxes and has been a player in the video-codec market. I assume that the company believes that it can usurp the network link.

In June, Tzero (www.tzerotech.com) announced a WiMedia product that supposedly works over coax. Presumably, UWB technology would handle the backbone requirement over coax and distribution within a room over the air. Then again, Tzero has previously claimed that its UWB technology could wirelessly distribute video around a home. In fact, I wrote an article on that possibility, although the company seems to be backing off those claims (see "UWB may yet serve whole-house video," www.edn.com/article/CA6345839).

I can't help but wonder whether the latest UWB noise is just a last-ditch attempt to salvage a problematic technology. UWB has surely seemed promising to investors and entrepreneurs alike. The media have extensively covered it. But no one has tamed it and brought products to market. Almost everyone has overhyped UWB and UWB-based Wireless USB. Artimi (www.artimi.com) is the only exception. In its UWB briefings, the company admitted that UWB would start to ramp up late this year and reach volume quantities in subsequent years. Artimi also seems more interested in linking portable devices at close range than in whole-home video.

Of course, there is also an incumbent video-over-coax technology in place. Entropic Communications (www.entropic.com) has led the charge in the MOCA (Multimedia Over Cable Alliance) standard to distribute video and other digital communications over currently installed coax in the home. Major service providers are now shipping MOCA technology. Entropic has just announced an upgrade in link rates over coax—from 100 to 180 Mbps. The UWB folks are again touting 480-Mbps rates, although they have yet to deliver. In reality, a solid 100-Mbps technology is all that's necessary to distribute multiple compressed HDTV streams, and 180-Mbps rates add more margin for error. Some UWB proponents tout specialty applications for handling uncompressed HDTV, but, if those applications exist, they are largely within a room and not across a home.

Meanwhile, *EDN* Senior Technical Editor Brian Dipert is at work on a new project comparing power-line, wireless, and other home-networking options. He tells me that the latest power-line technology works much better than previous offerings. Both he and I have had some troubles in the past testing that technology. This situation is an example of an application waiting for a technology that works. As a consumer, I'd run Category 5 wire in any home unless doing so was terribly inconvenient and expensive. Dipert recently found that a local fiber-to-the-home vendor in the Sacramento, CA, area had to install a new Cat 5 plant in his home to make IPTV work (see "SureWest: Initial Post-Install Fiber Details And Thoughts," www.edn.com/070705ed1). Certainly, that service provider would have preferred a no-new-wires approach to simplify the installation. Still, I'm hoping one or more no-new-wires technologies can deliver video. I'm not sure, though, that UWB is the one. **EDN**

Contact me at mgwright@edn.com.

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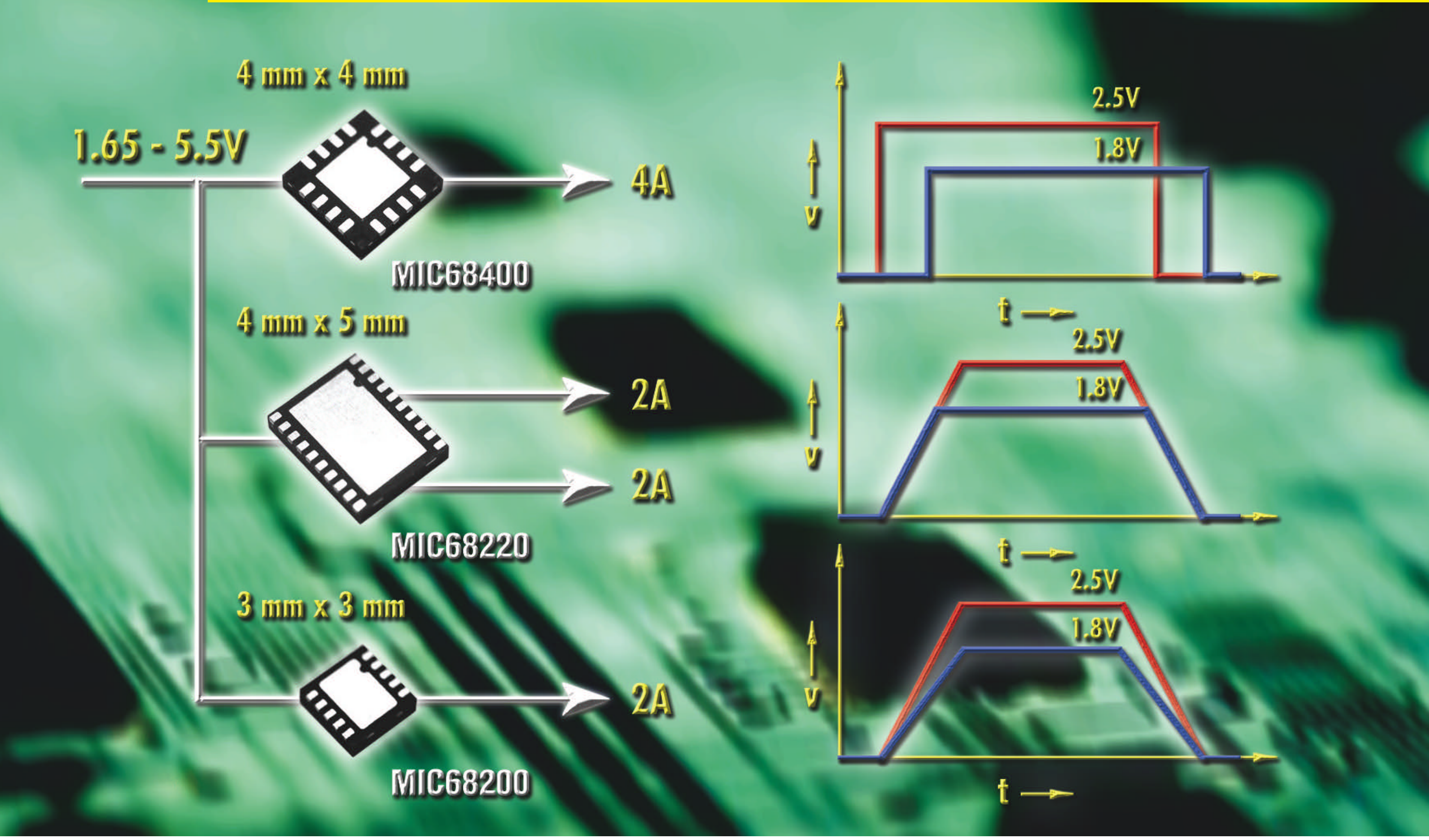

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Keeping Up With the Expanding Demands of High-Performance Audio

Application Note AN-1651

Joe Curcio, Field Applications Engineer

Engineers designing audio equipment for the high-end audiophile or professional recording markets have a limited selection of high-resolution signal amplifiers that will meet end-user demands for both outstanding objective and critical subjective performance. Suitable devices must provide a combination of state-of-the-art specifications for low noise and ultra low distortion along with high GBP and with unity gain stability. While nearly all suppliers develop and provide devices optimized for video, instrumentation, or low power, these applications demand a specification mix that does not necessarily align with the needs of the high-performance audio engineer. Accordingly, National has developed a series of high-performance, high-fidelity audio amplifiers specifically optimized for these applications.

The LME49710/LM4562 are representative of this group. Optimized for the high performance and professional community, they provide the designer with unprecedented levels of operation. Additionally, they can deliver an output current of ±26 mA into a 600Ω load, eliminating the need for a buffer with most headphone loads. Operating current is extremely low, serving the needs of both portable products as well as multimedia applications where multiple stages are used.

To meet the demands of the audiophile/professional community, a high-quality RIAA phono (moving-coil) pre-amplifier is designed using the LM49710. Note this design incorporates many of the ideas and philosophy generally embraced by the audiophile community as having both objective (measurable) and subjective (audible) merit.

Phono Amplifiers to Meet RIAA Standards

Magnetic phono amplifiers are needed to amplify and equalize the signals originating from magnetic phono cartridges to meet RIAA standards. The key parameters of concern with RIAA equalized phono pre-amplifiers are low noise, low total harmonic distortion, low intermodulation distortion and high GBP across the audio spectrum.

Although phono cartridge technology can be based on several forms of electrical generation, in some rare cases, the highest qualities are from electro-magnetic designs. These are using either fixed coil (moving magnet) or fixed magnet (moving coil) designs.

Moving magnet designs provide higher output voltages generally in the region of 1.0 mV for each cm/s tip of recorded velocity while moving coils deliver 0.1 mV under the same circumstances. Typically, reviewers agree that the moving coil configuration provides superior audible performance. This is most likely due to the lower mass of the magnet's cantilever assembly.

Table 1 shows the RIAA equalization response. The response is traditionally defined relative to 1 kHz with approximately 20 dB rise and attenuation relative to this frequency. The total dynamic range is actually greater than 40 dB as the high-frequency rolloff continues beyond the second high-frequency inflection point (2.122 kHz) which is beyond audibility.

Frequency	Amplitude	Frequency	Amplitude
20	19.3	800	0.7
30	18.6	1000	0
40	17.8	1500	-1.4
50	17	2000	-2.6
60	16.1	3000	-4.8
80	14.5	4000	-6.6
100	13.1	5000	-8.2
150	10.3	6000	-9.6
200	8.2	8000	-11.9
300	5.5	10000	-13.7
400	3.8	15000	-17.2
500	2.6	20000	-19.6

Table 1. RIAA Equalization Response

Power Supplies Can Affect Signal Fidelity

Although not commonly emphasized, a high Power Supply Rejection Ratio (PSRR) across the full signal bandwidth is critical to the audible performance of the circuit. Specifications widely discussed such as distortion, noise, and bandwidth are important to characterize the performance of the amplifier but it misses one critical area. If one envisions an audio amplifier as a device that modulates the power supply current into the load in direct response to the input signal, it is clear that the power

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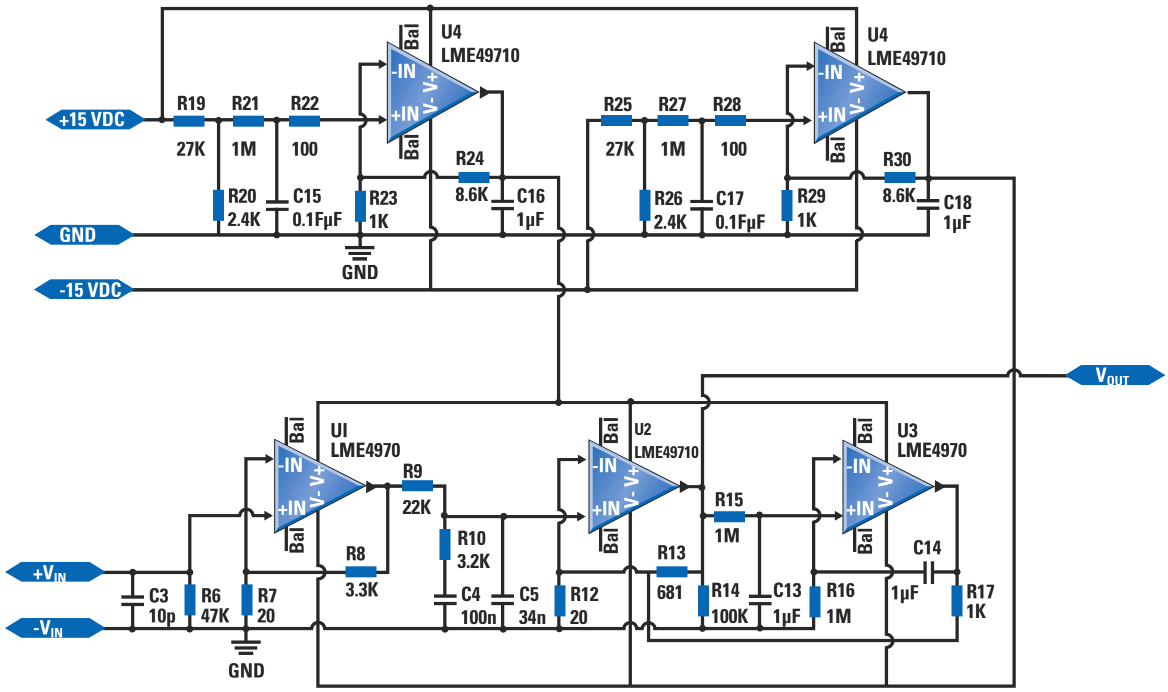

Figure 1. Passive EQ RIAA Schematic

supply rails must present a low and more importantly flat impedance across the audio bandwidth to preserve the audible spectral balance and overall integrity of the input signal. The PSRR of the LME49710/LM4562 is outstanding and characterized across the entire audio bandwidth and therefore is highly immune to power supply impedance discontinuities. However, given the low-level signals provided from moving coil phono cartridges, the effect is more pronounced and therefore the impedance of the supply rails is addressed in this application.

Figure 1 shows the circuit topology for a RIAA phono pre-amplifier with passive equalization capable of interfacing with a low output moving coil cartridge.

The circuit consists of two gain blocks separated by a passive RIAA equalization network. Gain distribution is defined by two issues – noise and input overload margin. To achieve the best noise performance, it is preferable to have high gain in stage U1 with the balance in stage U2. Alternatively from an overload perspective, the opposite distribution is preferred. By using high supply voltages it is possible to extend the gain of the first stage to 44 dB and minimize overload concerns especially with lower output moving coil cartridges. (If moving magnet cartridges are being used, it may be beneficial lower the gain of the first stage by 10 to 15 dB.) In order to meet a target mid band (1 kHz) gain of approximately 55 dB, the gain of the second stage has been configured to be approximately 30 dB (44 dB + 30 dB -20 dB at midband).

The network chosen to provide the RIAA equalization consists of components R9, R10, C4, and C5. The values shown are based upon the work of Lipshitz[1] and represent the nearest EIA standard values. More design details are online.

Note that it is possible to include a very low frequency roll-off response to reduce low frequency turntable noise from room or mechanical sources. The reader may incorporate this filter with the inclusion of a capacitor in series with R7. ■

To read the full version of this appnote visit edge.national.com

[1] Lipshitz, S.J, "On RIAA Equalization Networks," JAES Vol 27, No 6, June 1979, pp 458 – 481

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Lithium-ion batteries power next generation of electric vehicles

This year's Advanced Automotive Battery Conference, which took place May 16 through 18 in Long Beach, CA, offered four days' worth of technical papers analyzing the challenges inherent in adapting lithium-ion batteries, the favored battery technology for consumer-electronics portables. These batteries find use in automobiles, including EVs (electric vehicles) and PHEVs (plug-in-hybrid electric vehicles). PHEVs differ from the more common HEVs (hybrid electric vehicles), such as the Toyota Prius, in that the engine in PHEVs acts only as a backup if the user exceeds the mileage range. The PHEV battery requires daily charging for its primary power.

At the conference, JB Straubel, chief technology officer of Tesla Motors, presented "Development of Advanced Li-ion Battery Pack for EV and PHEV Applications," a paper explaining the advantages of using many small, individually fused, 18650-form-factor lithium-ion cells, rather than one large, prismatic battery, to make a battery pack. "It's easy to jump to the panacea of the new technology and forget the lessons [of] the past," said Straubel. "And we do have 10 years of a learning curve on lithium-ion [18650] cells." Lithium-ion batteries can cause thermal-runaway problems; Straubel pointed out that you can more easily handle catastrophic failures with small individual cells than with one large cell. Tesla claims impressive numbers for its pack: well-to-wheel efficiency of more than 135 mpg; energy storage of 56 kWhr; total energy density of 125 Whr/kg, fully tested, including vents and cooling; and an overall energy density for the entire car of 50 Whr/kg.

The Tesla Roadster EV relies on a battery pack employing about 6800 lithium-ion cells, enabling it to go from 0 to 60 mpg in 4 seconds, with a range of more than 200 miles.

Tesla engineers employed many pre-emptive procedures in designing for lithium-ion-battery safety, which Straubel passed on to attendees at the conference. For example, they warn, don't accept vendors' claims that they meet all safety standards; ask each vendor about its record and how long it has been in business. Also, assume that thermal runaway will occur, but design to prevent it. Include pack monitoring and protection and emphasize fuse design. Perform extensive testing, again emphasizing fuse testing. Finally, you should get third-party reviews from consultants, professors, and others.

Straubel did not specify Tesla's battery-pack secret for the car, which goes from 0 to 60 mph in 4 seconds and goes more than 200 miles between charges. However, he did reveal that Tesla is forming a subsidiary, Tesla Energy, in response to the many inquiries that the company claims it receives about its lithium-ion-battery-pack design. Despite the PHEV-inclusive title of Straubel's paper, Tesla's current road map calls only for EVs, leaving the door open for Tesla Energy to serve as a battery-pack designer for next-generation PHEV vendors.

—by Margery Conner

▷**Advanced Automotive Battery Conference**, www.advancedautobat.com.

▷**Tesla Motors**, www.teslamotors.com.

FEEDBACK LOOP

"Things are changing—and not in a surprising fashion, frankly. Programmability and customized programmable platforms—née customer-designed ASSPs (application-specific standard products)—are the new wave for a majority of systems houses."

—Steve Cox, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6449429. Add your comments.

Lattice offers 90-nm, flash-based FPGA

Lattice Semiconductor has announced its 90-nm, third-generation XP2 family of nonvolatile FPGAs, featuring preimplemented DSP blocks, along with twice the logic capacity and 25% greater performance than the previous generation. In 2005, the company introduced the 130-nm XP FPGAs, and, according to Gordon Hands, director of strategic marketing, Lattice has been diligently monitoring the device's use and customer suggestions for the features of a follow-on product. The new XP2, Lattice's first nonvolatile device in a 90-nm process, has better performance, higher capacity, and lower price per function than its predecessor, and it maintains reasonably low power for an FPGA.

The LatticeXP2 family comprises five members, with capacities ranging from 5000 to 40,000 four-input LUTs (look-up tables). The largest device has double the capacity of the largest device in the XP family. "We are using 90-nm technology, which is driving the cost of the device to 50% lower price per function, and we spent a lot of time focusing on the power," says Hands. Like the XP, the XP2 has a 1.2V operating voltage, but the new device has a 33% reduction in leakage power. Lattice stuck with 1.2V instead of going to 1V so that users could work with an operating voltage they are comfortable with and essentially swap out XPs with XP2s using the same power-supply circuitry.

With Xilinx (www.xilinx.com) recently jumping into the nonvolatile-FPGA market with its SIP (system-in-package) offering, Lattice now has yet another competitor in the market. But Hands claims that the single-chip, nonvolatile Lattice FPGAs offer better security, performance, capacity, and cost savings than SIP devices. With the single-chip XP2 device, Lattice employs FlexiFlash architecture. FlexiFlash preserves the benefits of the company's previous flash-based devices: single chips with an instant-on feature. The new devices employ Flashback, a new approach to on-die user flash, which allows you to back up the contents of enhanced-bit-rate memories within the device.

With the XP, design teams can upgrade XP devices in the field without downtime for either the device or the system it runs. Flashback is essentially an on-chip backup; for example, if a power outage or another type of interruption occurs during a field upgrade, the device automatically reverts to and runs the previous version of the device program. The device also includes as much as 885 kbits of block memory in 18-kbit, dual-port blocks. Designers can also convert LUTs into small, distributed-memory blocks to create small scratch-pad memories.

> "With the XP, design teams can upgrade XP devices in the field without downtime for either the device or the system it runs.

The XP2 family has as many as 12 preimplemented DSPs with pipelined MAC (multiply/accumulate) functions and as many as four PLLs (phase-locked loops) that allow designers to align and synthesize clocks in their designs. The family includes I/O capacities ranging from 86 to 540 pins and features flexible I/O-buffer support for popular I/O standards, such as LVCMOS (low-voltage CMOS), SSTL (stub-series-terminated logic), HSTL (high-speed-transistor logic), and LVDS (low-voltage-differential signaling). The buffers also support DDR2 memory interfaces at 400 Mbps, high-performance ADCs and DACs at speeds as high as 750 Mbps, and 7-to-1 LVDS-display interfaces at speeds higher than 600 Mbps. LatticeXP2 comes in CSBGA, FTBGA, FPBGA, TQFP, and PQFP packages.

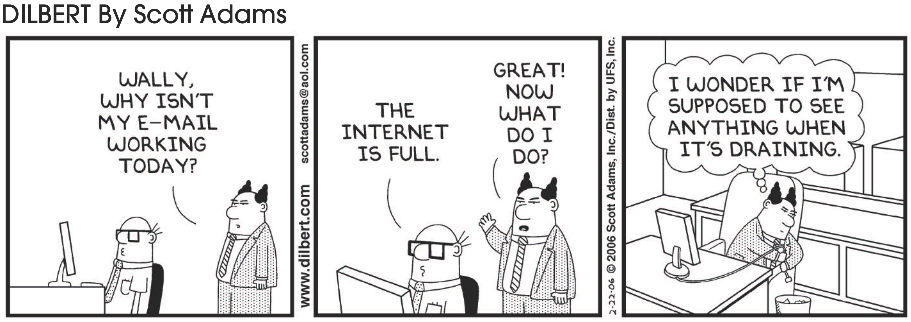
With the new device, the company has also improved its ispLever FPGA-programming software. It improves device performance by as much as 46%, with an average increase of 12%. The company has also reduced runtime by as much as 70% and an average of 30%. The new version, ispLever 7.0, also includes a new power calculator and the new Reveal logic analyzer. For $1495 extra, Lattice also offers the ispLever Pro IP (intellectual-property) bundle, which includes cores for DDR, DDR2, FIRs (finite-impulse-response) filters, FFTs, and triple-speed MACs.

Lattice is now offering samples of the first member of the LatticeXP2 family, the 17,000-LUT LatticeXP2-17, in 208-pin PQFP, 256-ball FTBGA, and 484-ball FPBGA packages. The company plans to bring the entire device family to market this year. Lattice expects the LatticeXP2-17 to sell for $12 (100,000) for delivery in 2008, and ispLever became available last month.

—by Michael Santarini

▷**Lattice Semiconductor**, www.latticesemi.com

DILBERT By Scott Adams



FEEDBACK LOOP

"Truly, the spirit of PT Barnum is alive and well in the audio marketplace."

—Paul Koning, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6418215. Add your comments.

Energy-harvesting conference covers cutting-edge and established technologies

The NanoPower Forum, which took place last month in San Jose, CA, was the first industry conference to focus on energy harvesting, the ability of a device to acquire and use energy from its surroundings and to eke out power from its environment. Topics included RF-power transmission and harvesting and storing vibrational, thermal, and piezoelectric energy. Designers look to energy harvesting to deliver a reliable source of power in extreme conditions for as long as 20 years—a capability that seems beyond the scope of small, price-competitive batteries. However, Lou Adams, regional manager for Tadiran Batteries (www.tadiran.com), pointed out at the conference that industrial- and military-grade lithium-thionyl-chloride primary batteries have lifetimes of more than 20 years, and they supply approximately 80 mAhr/year with a failure rate of only one per million cells. As a comparison, a microgenerator that generates power from machine vibrations might cost $200. Adams suggested that system designers compare that price with the price of a $2 Tadiran battery that might last for 20 years. The poster-child application for lithium-thionyl-chloride batteries is AMR (automatic meter reading), which requires infrequent, predictable transmission. Batteries are worth considering for applications with the same energy-usage profile of AMR.

Health issues arise as possible concerns about using RF-power transmitters as sources of wireless power. Regan Zane, PhD, of the University of Colorado—Boulder (http://ece-www.colorado.edu/~pwrelect) presented a paper, "Efficient low-power RF energy harvesting and power management," which compared radiation levels for common consumer appliances with the level of radiation you'd see in an RF-power transmitter. It found that a microwave oven or a cell phone emits 50 mW/cm^2 of leakage energy, a radar antenna emits 20 mW/cm^2, and a TV-station transmitter emits 10 mW/cm^2. On the other hand, an RF-power transmitter like the one that researchers at the University of Colorado built emits only 20 μW/cm^2, or about an order of magnitude less than the radiated energy levels you face in everyday life.

The power output and environmental hardiness of the technologies vary considerably, and the audience, which ranged from engineers to analysts, commented several times about the need for standards to measure the techniques. However, standards usually evolve after a silver-bullet application emerges to drive an industry, and the applications for energy harvesting are still too varied. Possible applications include wireless-sensor networks for industrial applications and patient monitoring. As health-care costs and an aging population make in-home monitoring an economical alternative to hospital stays, the ability to untether monitoring devices from the ac power mains makes energy harvesting an attractive feature.

—by Margery Conner

▷**NanoPower Forum**, http://nanopower.darnell.com.

07.05.07

DSC INCLUDES 32-BIT FLOATING-POINT INTEGRATION

Texas Instruments' new TMS320F2833x DSCs (digital-signal controllers) integrate a 32-bit floating-point unit that performs 300 MFLOPS (million floating point operations per second) with a 150-MHz clock rate. The inclusion of the floating-point unit increases computational performance for control applications by as much as 50% over previous devices. It also enables designers to avoid the effort of converting floating-point code into fixed-point code, as well as the effort of managing scaling, saturation, and adjustment of the numerical resolution of data when using a fixed-point implementation.

All F2833x DSCs include a 12-bit, 16-channel ADC that supports 12.5M samples/sec; a six-channel DMA controller; a single-cycle, 32-bit MAC (multiply-accumulate) unit; and as many as 18 PWM channels, of which as many as six support a 150-psec resolution. On-chip communication interfaces include CAN (controller-area network), I^{2}C, UART, SPI, McBSP (multichannel buffered serial port), and a user-configurable 16- or 32-bit external-memory interface. On-chip-memory options include 52 to 68 kbytes of RAM and 128 to 512 kbytes of flash. The devices include two QEP (quadrature-encoder-pulse) and as many as six event-capture interfaces.

The initial three devices will become available for sampling in September for $13.30 to $19.95 (1000), and they will be fully AEC (Automotive Electronics Council, www.aecouncil.com) Q-100-qualified for automotive applications. TI schedules volume production for the second quarter of 2008. The F2833x controllers are fully software-compatible with all previous TMS320C28x controllers, and the Code Composer Studio integrated development environment will support software development for the F2833x controllers. Developers can start programming today using IQ Math, a virtual-floating-point-software library that works with any F28x-based eZdsp development tool. Software written with IQ Math automatically runs on the F2833x controllers. The C2000 digital-motor-control- and digital-power-supply-software libraries will also support the F2833x devices.

—by Robert Cravotta

▶**Texas Instruments, www.ti.com.**

Breker has a plan for better IC verification

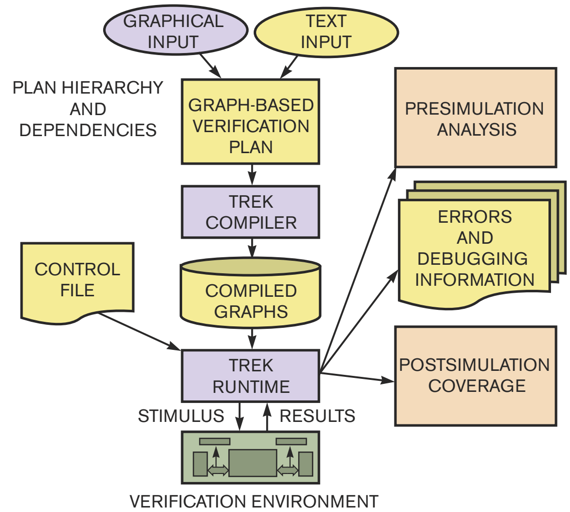
EDA start-up Breker Verification Systems wants to help you reduce the amount of testbench generation and overall verification you need to do. The company aims to help you create a comprehensive IC-verification plan up-front in the functional-verification process and to help you drive better test vectors into your current verification environment. The company calls its first tool, Trek, a graph-based functional-test-synthesis technology.

Breker founder Adnan Hamid, formerly of AMD (www.amd.com) and Cadence (www.cadence.com), developed cell-characterization technology while at AMD. Hamid notes that designers spend two-thirds of the design process doing verification and claims that, for every line of RTL code, verification engineers must write 10 lines of verification-testbench code to check that it is functionally correct. Over the years, he's discovered that a lack of effective planning has caused much of the verification problem. "We have not come up with any rational way to think about how to plan to verify a design, how to capture that plan in some form that is understandable, and then how to get from that [plan] to execution," says Hamid. Many teams today typically create a spreadsheet plan, essentially a laundry list of things that require testing. That method is often error-prone and ineffective. Other design groups have no organized plan, instead using a "spray-and-pray" method in which they simply apply constrained random-test generation using an automated testbench tool. "That whole story is: Throw random numbers at your design and hope that it hits all the corner cases, and, if it doesn't, then come back and spend a bunch of time incrementing functional coverage points," says Hamid. His idea with Trek is to help engineers start with the end goal and the end function of the design in mind and then create a plan to meet that goal.

Breker applies dependency resolution to graphs, which constrains what a graph can do. "Once you've combined dependencies with graphs, you can come up with a process to construct a verification plan that says, 'Start with the outcome that needs testing and then break that [outcome] down step by step to think about what inputs you need to test that outcome,'" he says. This approach lets you express complex verification plans with little code. "We are seeing a 10-times or better reduction in the amount of code we need to write to come up with a graph-based plan versus a traditional testbench," Hamid says.

Users feed Trek text-based source code or a graphical file—verification IP (intellectual property) or subgraphs that Breker or the user develops. They then create a plan hierarchy and dependencies. "Once you have a graph, you can do presimulation analysis to see what portions of the graph are reachable and where you are going to spend your verification time, given the way you've written the plan, and you can estimate how much simulation you will need to run to get coverage of the plan," he says.

After running those steps, the tool then generates functional-test vectors to run in the verification group's environment. "We not only generate input stimulus for the design, but also check that the resulting outputs are correct," says Hamid. This feature is important for directing random-test generation and for helping users know whether they have done enough verification. "When you use a graph-based verification plan and you start out thinking about the outcome you want to test and start solving for the inputs that will give you that outcome, you know the outcome, so checking is straightforward." With the plan as a graph, you can traverse the entire plan with 100% coverage. It takes 100 to 500 simulation cycles to achieve this coverage, depending on the size of the design.



Breker's Trek allows users to create a verification plan to make better test vectors for their IC-verification projects.

The tool displays the verification plan in a graph that illustrates hot spots, showing what areas of the design have coverage. "It's a quick way to dive in and say, 'Why haven't we reached this node? Is there a dependency that kept us out of there, or did we not run enough simulation?'" Once you find a hot spot, you then check on whether you incorrectly described a graph or dependency or whether you did too little simulation. If neither is the case, an error in the design is likely the cause. You can then go back to your verification environment and home in on that section of the design to solve the problem.

The company currently offers subgraph modules for TCP/IP (Transmission Control Protocol/Internet Protocol), RDMA (rate-division multiple access), SSL (Secure Sockets Layer), Fibre Channel, SONET (synchronous optical network), and PCIe (Peripheral Component Interconnect Express). Users can add these subgraphs to their larger graph-based verification plans. The tool can also interface with third-party-IP bus-functional models for the generation of test cases. Prices for the tool start at $32,000 for an annual subscription.

—by Michael Santarini

▷**Breker Verification Systems Inc**, www.brekersystems.com.

VOICES

Texas Instruments' Gene Frantz: bringing ideas to life

Gene Frantz is the principal fellow at Texas Instruments, a manufacturer of analog-, DSP-, and DLP (digital-light-processing)-chip technologies. Frantz identifies emerging opportunities that could benefit from digital-signal processing and works as a liaison between the new ideas and the technologists that bring them to life. *EDN* asked him a few questions about the benefits of semiconductor companies' doing systems design instead of just chip design.

What is the crux of the issue for semiconductor companies grappling with how to best be a component supplier, a system-IC vendor, or both?

A With current semiconductor technology, we can put a complete system on a chip. At the same time, it has become so complex and difficult to do this task that you have to be a semiconductor person to know how to put that system on a chip. With these two points in mind, either we as a semiconductor company learn how to be more of a systems company, or our system customers will learn to become semiconductor houses. As a result, our goal should be to be one of two things: either a systems house that does IC design or a component house that understands systems.

At TI, we are a component company that is learning to understand the system so we can be conversant with our partner customers. We have to have enough systems knowledge to interpret what our customer wants to be effective in making the components they need. At the end of the day, we sell semiconductor components and subsystems.

What effect does this approach have on your system-level offerings?

A When we introduced the [TMS]32010, it was a DSP for all markets. If you look at our product line now, you will see we no longer sell a DSP; we sell vertically targeted components that are DSP-enabled. As an example, our DaVinci and OMAP [Open Multimedia Applications Platform] product lines are positioned as vertical-market platforms rather than as ICs, which means we also provide a good development environment, software libraries, and a network of partner companies that can help fill in the gaps. We're broadening our definition of semiconductor components to include software components because they go hand in hand. The targeted-platform approach greatly expands the number of people that can innovate from a few experts with assembly and domain expertise to a much larger group of developers that know C programming and have an understanding of their target domain.

How does taking on a systems approach help encourage innovation by your customers?

A My customers want four things from me: a device that is low-enough cost, low-enough power dissipation, and high-enough performance to be first to market. In fact, skip the first three; just get me to market first. When a system product is initially introduced, it has three components to its value: hardware, software, and time to market. At maturity, its value is based only on the hardware. A lower cost of entry and a fairly quick time to market increase the opportunities for developers to try their ideas and allow the market to choose the good ones.

The only part of Moore's Law that is still applicable is the original part about doubling the number of transistors. This growth rate allows us to be financially efficient with the "sloppy" use of transistors to enable everything to be programmable while delivering higher performance at lower cost and power. This [situation] is leading to the condition that what ties down the circuit is the software rather than the hardware. Recognizing this [fact], we grapple with whether we should sell software as hard-coded components that you cannot modify or whether we should sell source code. When the software is new and scarce, it has high value, but that value drops the more widely it is used.**—by Robert Cravotta**

BY BONNIE BAKER

Transimpedance strikes again

Multiplying DACs (MDACs) and their postamplifiers bridge the digital and analog worlds. MDACs generate a current proportional to an input digital code (**Figure 1**). The postamplifier converts the DAC's current-output signal to a voltage level. A simple current-to-voltage conversion seems easy to implement with a DAC, amplifier, and resistor. However, this circuit presents stability issues.

For the application, the output model of the MDAC contains a variable current source, resistor, and capacitor (**Figure 1a**). The value of the output resistance and capacitance depends on the input code to the DAC. In general, programming the MDAC to zero scale causes the output resistance, R_D, to be near infinite. When you program the DAC to full-scale or all ones, this resistance is equal to the feedback resistance, R_F. (See the manufacturer's data sheets.) The DAC's output capacitance, C_D, also varies with input code according to the number of internal gate-source junctions across the MDAC output. At full-scale, the MDAC output capacitance equals the data-sheet specification. At zero, the MDAC output capacitance is equal to about half the full-scale value. For stability calculations, use the full-scale output values of R_D and C_D.

The second subnetwork is the amplifier-feedback network. To maintain precision, most MDACs have a feedback resistor on-chip. The feedback capacitor, C_F, is discrete.

Finally, op amps have a range of specifications, but only a few affect the MDAC circuit's stability: unity-gain bandwidth, f_U; input differential capacitance, C_{DIF}; and common-mode capacitance, C_{CM}.

In this system, total capacitance at the amplifier input is equal to $C_{IN}=C_D+C_{DIF}+C_{CM}$. In **Figure 1b** and **1c**, the closed-loop zero is equal to $f_1=1/(2\pi(C_{IN}+C_F)(R_D||R_F))$. The closed-loop pole is equal to $f_2=1/(2\pi C_F R_F)$.

You ensure system stability if the rate of closure between the open- and closed-loop-gain curve equals 20 dB/decade. To do so, select an amplifier with unity-gain bandwidth of less than f_1 or greater than f_2.

It is easy to design a stable circuit if f_1 is higher than the amplifier's bandwidth:

$$C_F \geq (1+\sqrt{(1+8\pi C_{IN} R_F f_U)})/2\pi R_F f_U.$$

Alternatively, if f_2 is lower than the intersection of the open- and the closed-loop-gain curve, use:

$$C_F \leq -C_{IN}+1/(2/\pi(R_F||R_D)f_U).$$

Use these calculated values of feedback capacitance as starting points for your test circuit. Circuit parasitics, device-manufacturing variations, and other factors can encourage you to modify the feedback-capacitor value.

Stabilizing the MDAC's analog signal is critical. However, also consider amplifier noise, input bias current, offset voltage, MDAC resolution, and glitch energy. EDN

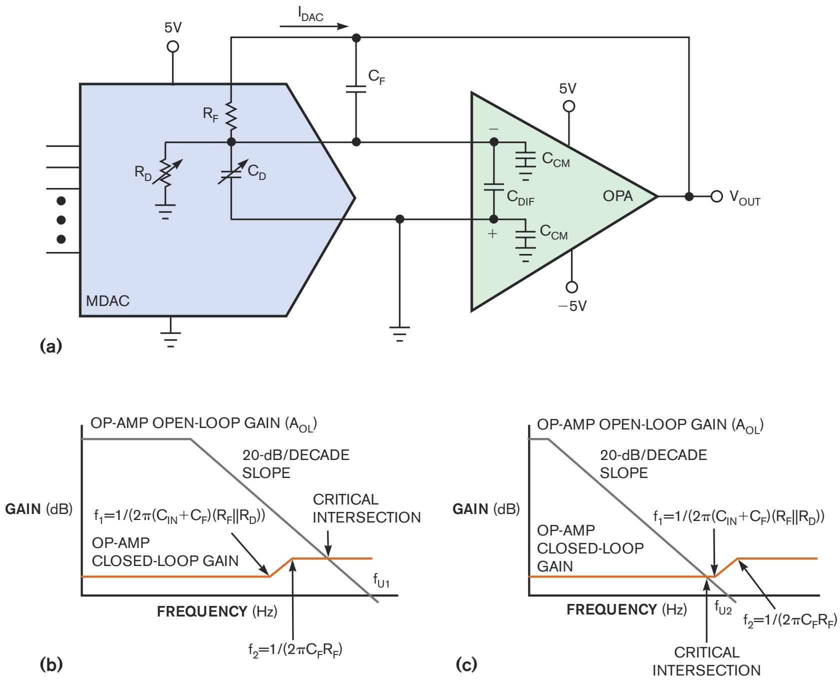
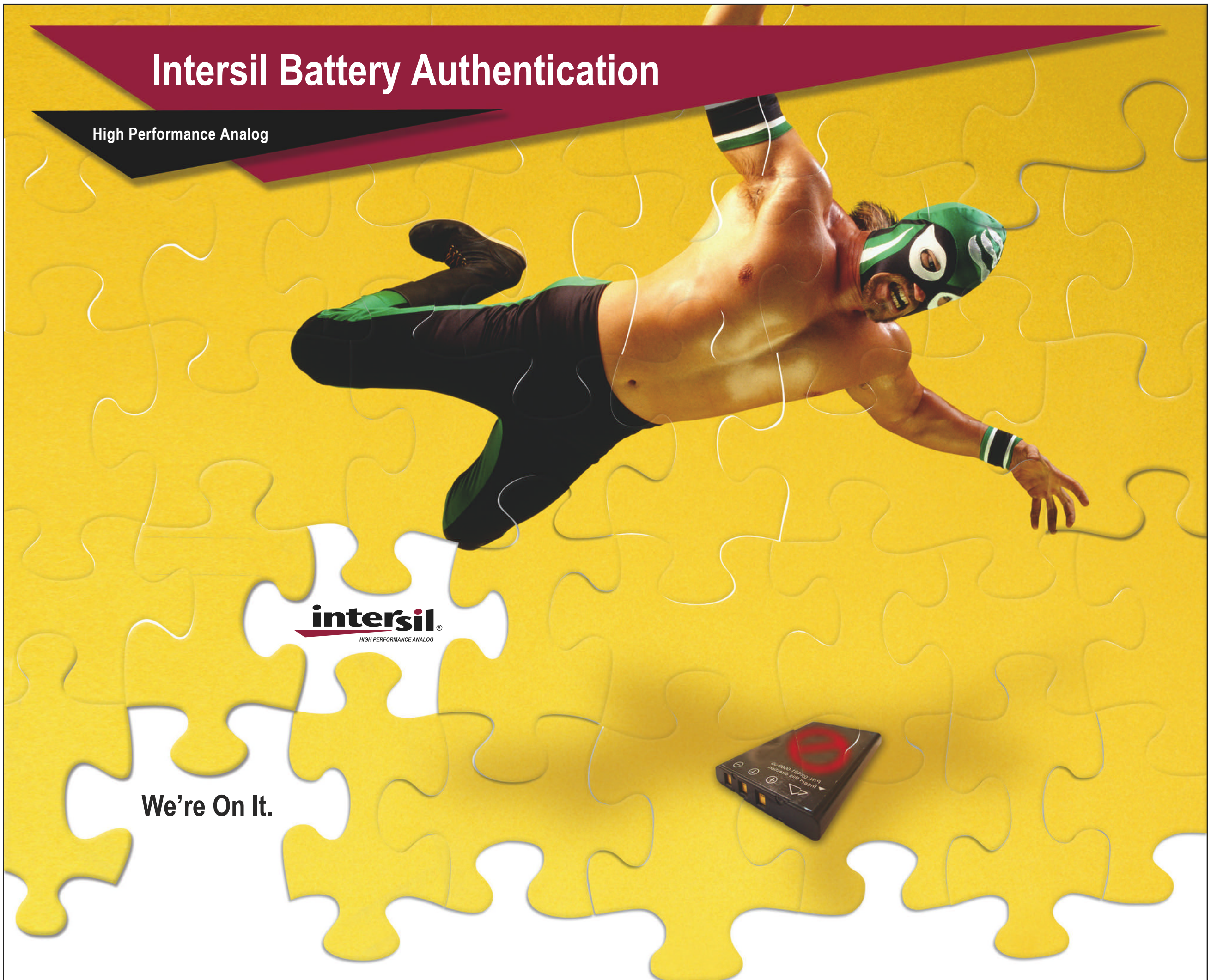


Figure 1 An MDAC output model (a) has a current source, resistor, and capacitor. Frequency responses use high- (b) and low-bandwidth amplifiers (c).

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

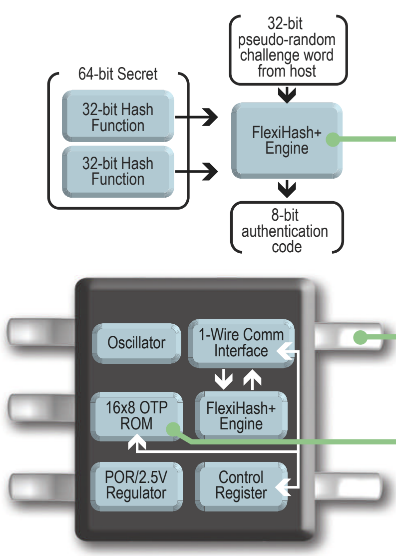


Intersil's **ISL9206 FlexiHash+™ Engine delivers high-security battery authentication** at a low cost.

Intersil's ISL9206 is an easy-to-use, robust, and inexpensive battery authentication solution for 1-cell Li-Ion/Li-Polymer or 3-cell NiMH series battery packs.

ISL9206 Key Features:

- Challenge/response-based authentication scheme using 32-bit challenge code and 8-bit authentication code.
- FlexiHash+ engine uses two sets of 32-bit secrets for authentication code generation.
- 16x8 one-time programmable ROM memory.
- Additional programmable memory for storage.



Patent pending FlexiHash+ engine consists of four separate programmable CRC calculators. Two sets of 32-bit secret codes are used for authentication code generation.

XSD single-wire host bus interface communicates with all 8250-compatible UARTs or a single GPIO pin. Supports CRC on read data and transfer bit-rate up to 23Kbps.

16 bytes of one-time programmable ROM memory for storage of pack information and ID, device authentication secrets, device default settings, and factory-programmed trim parameters.

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RECEIVING ELECTRICAL POWER WITHOUT THE USE OF WIRES HAS LONG BEEN AN IDEAL FOR ELECTRONIC DEVICES. HOW FEASIBLE IS IT, AND WHAT ARE SOME OF THE OTHER OPTIONS?

POWER WITH NO STRINGS ATTACHED

BY MARGERY CONNER • TECHNICAL EDITOR

Any technology that offers to free applications from power cords and wall warts will confer a definite salable edge on electronic devices. Applications that would benefit from wireless power range from portable consumer electronics, such as cell phones and MP3 players, which could jettison their wall warts and power adapters, to low-power wireless-sensor networks, which could be free of frequent battery replacement, to medical implants in patients who could avoid surgery to replace batteries.

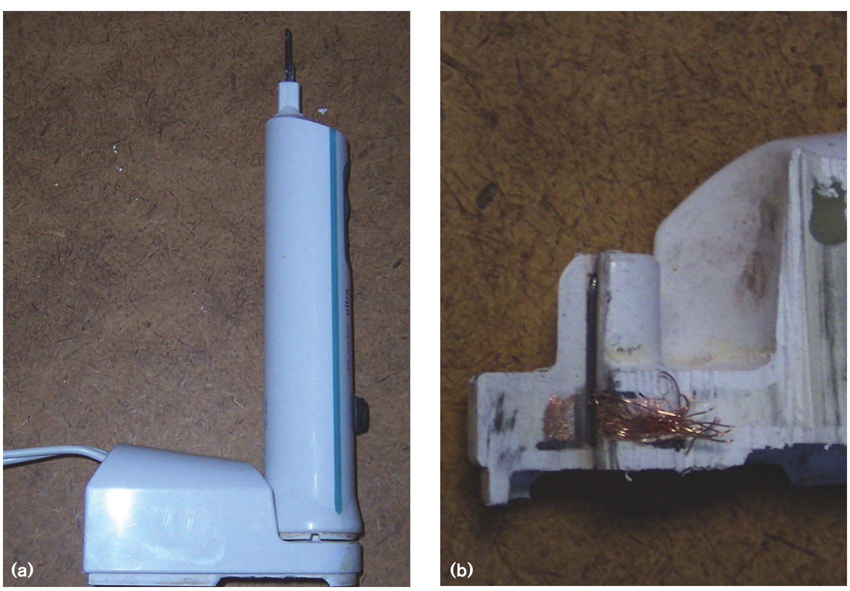

Figure 1 In this rechargeable electric toothbrush, no conductive contact occurs between the toothbrush holder and the charging unit. Energy transfer takes place through inductive coupling (a). This cutaway of the encapsulated base shows the primary winding of the transformer, with a ferrous rod pushing into the key that the toothbrush unit fits onto. Precise alignment is necessary to maximize the coupling between the two windings (b).

But how close are we to having a practical replacement for power cords, and what are the various options? What are the constraints these options imply in power levels, frequencies, and device placement? And, does power at a distance pose any health risks?

One wireless technology, inductive coupling, is familiar to anyone who has a rechargeable electric toothbrush, which has no conductive contact with its charging unit (**Figure 1a**). The charging unit, which is connected to ac wall power, has the primary side of a transformer in its base, with an iron center that keys into the secondary side of the transformer, which resides in the handheld toothbrush. After you brush your teeth, you typically remove the brush from the end of the brush unit and place the brush unit on the charging base. The brush unit, which an iron-cored key holds in place, fits perfectly over the primary. This key fits into the hole through the center of the secondary in the brush unit (**Figure 1b**). This keyed arrangement makes the physical alignment of the primary and the secondary coils fixed in the x, y, and z planes. This precise alignment is necessary; if the primary and secondary misalign by a fraction of an inch, the power transfer becomes inefficient. Cell-phone manufacturers could use a similar arrangement for recharging rather than rely on a charging unit. However, the transformer secondary is too bulky for consumer devices that must fit into a purse or a pocket, rather than spend their lives on a bathroom counter. And the primary reason the toothbrush holder uses the inductive power coupling is not for ease of connection, but because the holder's wet environment necessitates the sealed aspect of the power coupling.

To avoid the inductive coupling's constraints of close, precise alignment, eCoupled has introduced "adaptive-inductive coupling," in which the power circuit senses any change from the optimal positioning of the two coils and then looks for the best operating point for that configuration. The circuit's load shift causes the impedance and, thus, the resonant frequency of the circuit to change. In addition, eCoupled adds a digital-control loop to respond to changes in the load beyond the transformer coupling device. According to Dave Baarman, director of advanced technology for eCoupled, this combination of adaptive inductive coupling and a digital loop means that the power circuitry can maintain power to a device even when the device moves as much as several inches in the x and y planes and slightly less than an inch along the *z* axis.

SKIN DEEP

But this less-than-an-inch constraint isn't as limiting as it first sounds. "The distance [in the *z* axis] you need is just the 'skin thickness' you have on your MP3 player or cell phone," Baarman explains. That's enough to be able to casually place a device in a charging region on a counter top. Magnets enable you to feel when a device is aligned in a charging spot, ensuring alignment in the x and y plane—the counter top. The company has announced adaptive-inductive-coupling licensing partnerships with companies such as Motorola, Visteon, and Herman Miller, although these companies haven't announced any adaptive-induction-coupling-based products. Herman Miller will be making such announcements by early 2008, however, according to Mark Sherman, the company's corporate communications manager. The technology does have a track record: eCoupled's sister division, Fulton Technologies, has since 2002 used adaptive-induction coupling to power the electronics in its water-purification system. Baarman claims that eCoupled has tested adaptive-inductive coupling at power as high as 1400W.

AT A GLANCE

- Recent work in wireless power has focused on inductive coupling and RF transmission.
- Inductive coupling offers more than 1 kW of power, but range is on the order of an inch or less.
- RF transmission has a range of 30 feet but at power levels of less than 100 mW.
- Battery technology has improved battery life and failure rates for industrial- or military-grade batteries, so batteries may also be options for wireless power.

The trade-off of inductive coupling is that it has a relatively high power level but a small range. For some applications, such as wireless-sensor networks, you may be willing to forgo high power for a greater power-transmission range. Transmitting RF energy may be a consideration for these applications. Powercast has developed the Powercaster transmitter and Powerharvester receiver chips operating at 900 MHz, through which you can broadcast and receive energy (**Figure 2**). Their range is several meters, and the power level is as much as 100 mW. This low power level may not be the restriction it seems: If your device, such as a node on a wireless-sensor network, has periods of higher power needs followed by long sleep states, consider adding batteries to the device and use the RF-power receiver to trickle-charge the unit. The devices sell for less than $5 each (production volumes).

An example of the devices' use in wireless-sensor networks is a temperature- and humidity-monitoring network in the penguin exhibit at the Pittsburgh Zoo and PPG Aquarium (www.pittsburghzoo.com). In this cold, wet environment, no power was available, and the exhibit's developers could not bring in cables. They originally set up the sensor network with alkaline batteries to power the nodes, but the batteries wore out within weeks. Powercast retrofitted the nodes with Powerharvester receivers and power circuits and placed a Powercaster transmitter with a patch antenna on the ceiling of the exhibit about 30 feet away from the receivers. Every two minutes, a pulse from the transmitter wakes up the sensor nodes, which reply with temperature, humidity, and state-of-charge information. They then return to a sleep state. They continuously charge from the transmitted RF power, however, keeping the rechargeable alkaline batteries at a constant 3V.

SAFE POWER LEVELS

The Federal Communications Commission's Office of Engineering and Technology Bulletin 65 governs RF-safety issues, according to Keith Kressin, Powercast's vice president of sales and marketing. The bulletin tells you how much power is allowable for a device that sends out RF (**Reference 1**). A microwave oven has leakage levels of 50 mW/cm^2, about the same as a cell phone's radiated RF energy. TV/radio transmitters emits 10 mW/cm^2, and an RF-power transmitter emits about 20 $\mu W/cm^2$—far less than levels that are common in everyday life (**Reference 2**).

Energy harvesting of ambient RF power is another possible option for RF-power transmission, but, just as there's no such thing as a free lunch, you should be cautious when estimating the power available from RF energy. Zoya Popovic, PhD, a professor of electrical and computing engineering at the University of Colorado—Boulder (http://nemes.colorado.edu/microwave), suggests that you keep

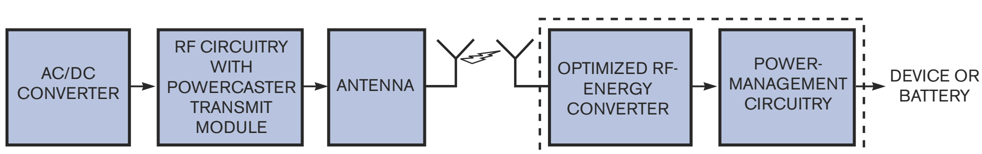

Figure 2 The Powercast RF-transmission platform comprises a Powercaster transmitter and a Powerharvester receiver. The power output is less than 100 mW, but that amount is sufficient to charge an internal battery in a wireless-sensor node or even a small, handheld consumer-electronics device.

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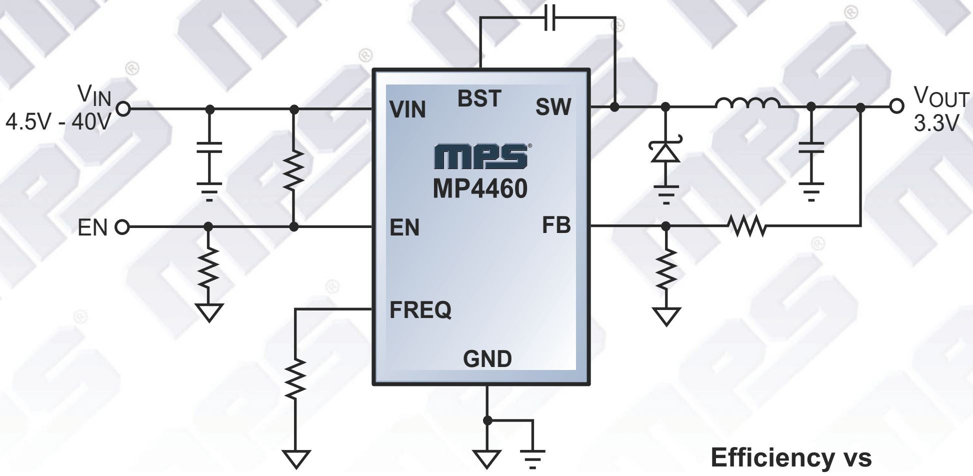

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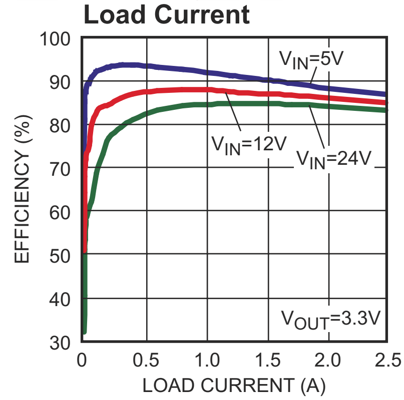

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HIGH-EFFICIENCY RF-RECTENNA DESIGN

By Hubregt J Visser, J Theeuwes, M van Beurden, and G Doodeman

A "rectenna" is a rectifying antenna. At its simplest, it comprises a Schottky diode and an antenna and converts the RF power it receives at the antenna into dc voltage. The challenge is how to maximize the power-conversion efficiency of rectennas for input-power levels of, for example, 0 dBm or less. We employed a method of directly conjugate-matching a rectifying circuit to a microstrip-patch antenna, so that the need for a matching network between the two no longer exists, and the rectenna's efficiency improved. This matching technique automatically suppresses the reradiation of harmonics by the microstrip-patch antenna, because the harmonics will be mismatched.

A PCB (printed-circuit-board) layout of a traditional planar-microstrip rectenna with a probe-fed antenna shares a common ground plane with a microstrip network (Figure A). With the aid of analytical models for the antenna and the rectifier, we designed single-layer, internally matched and filtered PCB rectennas with low input-power levels.

We analyzed the rectangular microstrip-patch antenna with a cavity model. A newly developed effective length and width take care of the fringe fields of the microstrip-patch antenna. A fourth-order Runge-Kutta routine solved for the packaged diode voltage and the generator current. An FFT then transformed these time-domain parameters to the frequency domain, in which, for each harmonic, a packaged diode impedance was determined for a fixed incident-power level.

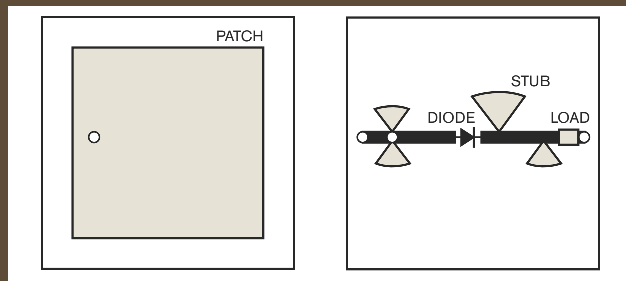

Figure A A PCB layout for a planar microstrip rectenna with a probe-fed antenna and an impedance-matching and filtering network shares a common ground plane with a microstrip network.

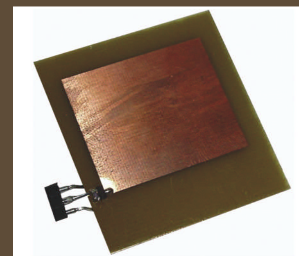

Figure B The newly developed, 28×31-mm rectenna is more compact, uses a single-layer PCB, and has an efficiency of 52%.

After finding the complex diode impedance, we determined the microstrip-patch edge's feed point to obtain the conjugate impedance of the diode and thus a conjugate match between the antenna and the diode (Figure B).

With the developed analytical model, you can accurately determine the rectenna output voltage as a function of input power at the antenna (Figure C). This design realized an efficiency of 52% for 0-dBm input power at 2.45 GHz, showing an improvement of more than 10% over a traditional rectenna design (Reference A). A series connection of these rectennas power a standard household wall clock at a distance as long as 6m (Figure D). The eventual applications, however, will be in charging batteries at a distance.

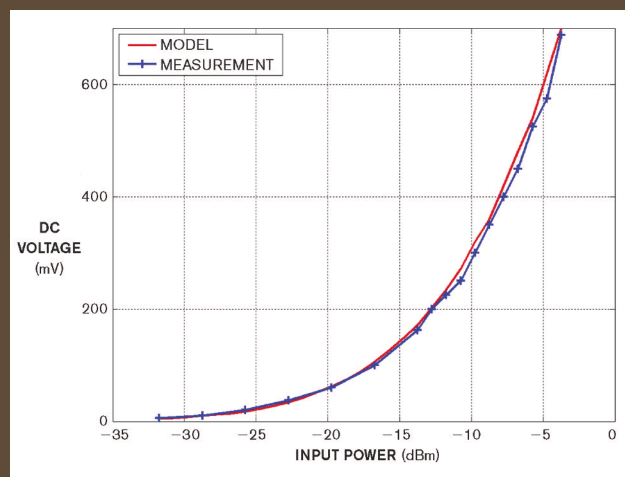

Figure C The rectenna's output voltage is a function of power incident upon the antenna.

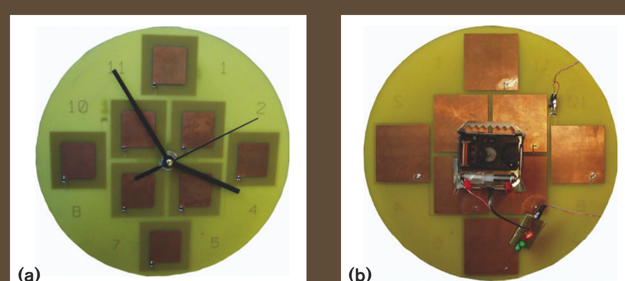

Figure D Eight 2.45-GHz rectennas in series power an electric wall clock (a). The back view shows a voltage-protection circuit (b).

Authors' biographies

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these three points in mind: First, ambient power covers a broad range of frequencies. The best way to gather RF energy is to design an antenna and power circuit for that frequency; you need to have an antenna and power circuit that can work in that environment, which means it has to be broadband or at least multiband.

Second, when harvesting ambient RF, you have no idea how the electromagnetic wave is polarized. Popovic gives an example: "If you transmit from one corner of the room a vertically polarized wave with a wire antenna, by the time the energy bounces around the room and arrives at the other side, the power will be equally distributed in both the horizontal and the vertical polarization. If you want to capture that [power] efficiently, you must design for both polarizations."

Third, because of the multipath environment, the power at the RF receiver varies not only in frequency and polarization, but also in power level. Popovic's team designs RF-power-receiver circuits having "rectennas," antennas with rectifying circuits that produce dc voltages. As the power level varies, so does the dc voltage at the output of the rectenna. Because energy-storage devices, such as batteries and capacitors, cannot tolerate wide voltage swings, the team placed a power-management and -buffering stage between the rectenna and the energy-storage component (see **sidebar** "High-efficiency RF-rectenna design").

Another technology, although not contactless, is Wildcharge's wire-free development. A Wildcharge-enabled device contacts a charging pad through an ohmic contact—a sputtered metal pad produced through a photolithographic process—to charge a cell phone or a similar consumer device. Wildcharge plans this summer to introduce a 15W, $40 charging pad that can charge multiple low-power devices. Devices will require an adapter to use the pad, but they can also have built-in Wildcharge technology and charge from any Wildcharge pad.

New wireless-transmission technologies are still in the research phase. Massachusetts Institute of Technology (www.mit.edu) physicist Marin Soljacic has announced "nonradiative-resonant-energy transfer" for distances of less than a few meters. The technology relies on copper coils tuned to resonate in identical magnetic fields (**Reference 3**). In addition, researchers at the University of Tokyo (www.u-tokyo.ac.jp) have developed a four-layer plastic sheet with printed coils, organic transistors, and MEMS (micro-electromechanical-system) switches that use inductive coupling to power devices fitted with receiver coils (**Reference 4**). Both of these technologies are still un-

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dergoing research, and commercialization is at least a few years away.

But even the approaches from eCoupled and Powercast are still new and have potential drawbacks and unknowns. Keep in mind that battery technology has also advanced. All batteries are not created equal, and the alkaline rechargeable battery with a lifetime of less than a year is not your only option for charging a low-power device. For example, Tadiran claims that its industrial- and military-grade lithium-thionyl-chloride batteries have a lifetime of more than 20 years and a failure rate of fewer than one cell per million. These primary, nonrechargeable batteries have low leakage current and high energy capacity. Tadiran's AA-sized high-power lithium battery, for example, has a nominal voltage of 4V compared with the 1.5V of a consumer device's AA battery. The high-power unit also has an available net capacity per cell of more than 2 Ahr. The battery will last more than 20 years powering a system that consumes power at 81 mAhr/year with an end-of-life voltage of 3V. These batteries cost less than $10 each, or less than 50 cents per year. Consider whether an industrial-rated battery will serve your design before venturing into more expensive new technologies. EDN

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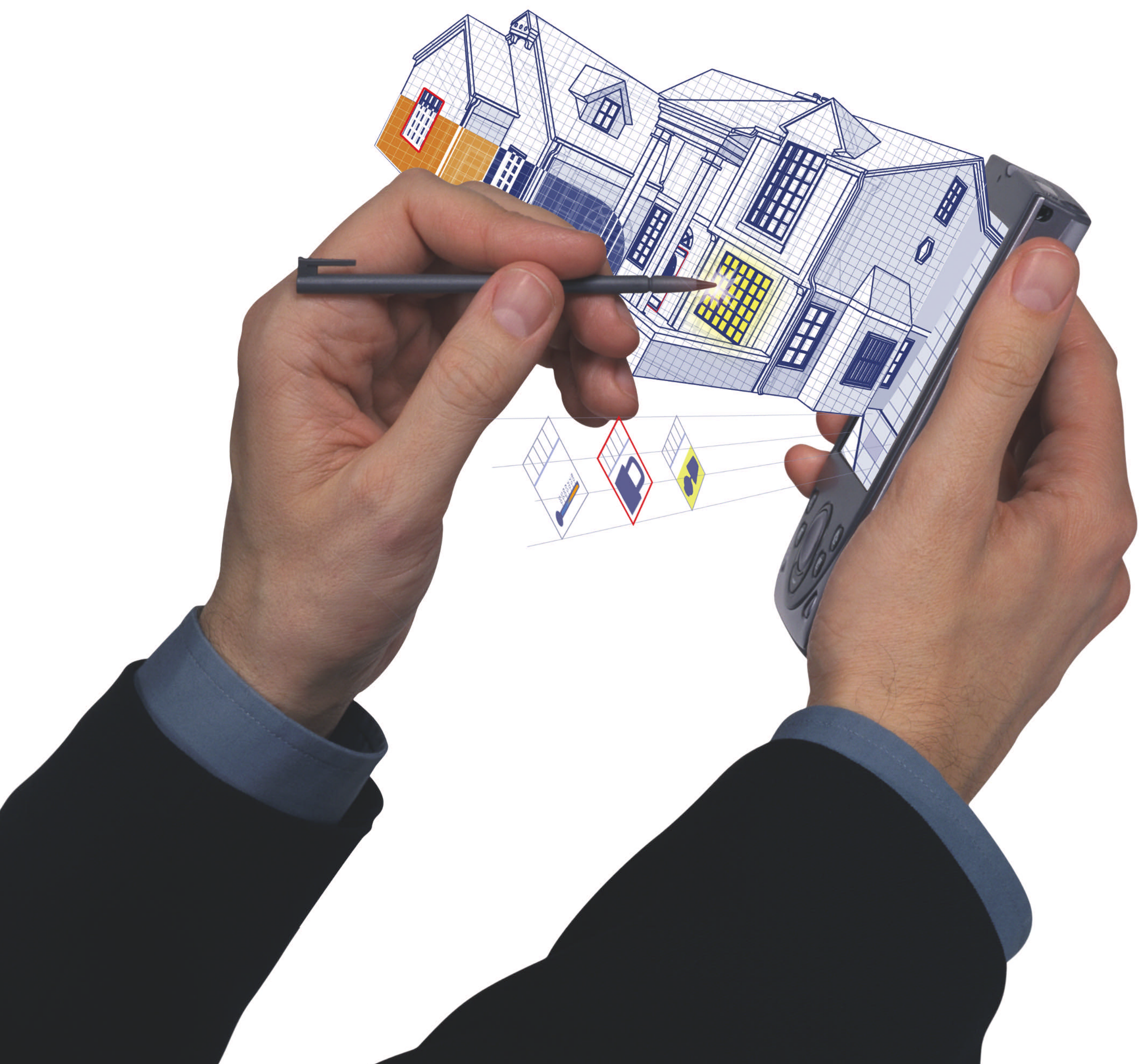
Networking moves to home automation

BY RICHARD A QUINNELL • CONTRIBUTING TECHNICAL EDITOR



AFTER LANGUISHING FOR YEARS, HOME AUTOMATION IS SEEING A SURGE OF ACTIVITY AS NEW TECHNOLOGIES, EMERGING STANDARDS, AND THE NETWORKING OF CONSUMER DEVICES CONVERGE TO DEVELOP THE INTELLIGENT RESIDENCE.

The dream of an intelligent home that automatically controls the living environment and responds to individual preferences has been around since the advent of the microcontroller first suggested the possibility. High cost, reliability issues, limited capability, and a lack of standards have imposed major constraints on the market, however, keeping home automation more in the realm of imagination than practice. The advent of wireless technologies, the emergence of home-networking standards, and pull from both the entertainment and the energy markets are now revitalizing efforts to realize that dream, although industry participants are still hotly contesting the implementation methods.

The first attempts at home automation provided only simple remote control of basic functions, such as turning lights, fans, and appliances off and on. The X10 power-line-signaling technology, which Scotland's Pico Electronics first developed in 1975, is typical of these early attempts. The X10 control system sends data at 1 bit/8.33 msec, is limited to 16 commands, and can control a maximum of 256 devices in a single network. Despite these limitations, however, X10 products have enjoyed limited but continuous success in the market and are still available for consumer purchase and installation.

To provide more powerful and comprehensive control functions for home use, the EIA (Electronic Industries Association), now the CEA (Consumer Electronics Association), began in 1984 developing a set of standards for a common command language that would handle a variety of devices. The effort also defined communications methods for many media, including twisted-pair wiring, infrared, RF, and power-line signaling. The resulting CEbus standard, which the industry adopted in 1994 as EIA-600, targeted remote control, remote instrumentation, security systems, energy management, and entertainment coordination with other wiring that carried the entertainment content.

Unfortunately, the CEbus proved to be too much, too soon. It was costly to implement, appeared before the consumer market had been exposed to the Internet and the concept of networking, and did not gain widespread support. What support it had gradually faded. CEbus-product vendor Domosys Corp, for example, eventually abandoned the CEbus in favor of its proprietary PowerBus networking technology. The CEbus industry organization's Web page, www.cebus.org, is now inactive.

Other technologies arose for home networking, with one of the most successful being the LonWorks platform from Echelon. LonWorks targets not only home automation, but also industrial and au-

tomotive control, in which it has seen greater success. Several industrial and building standards, including ANSI/EIA709.1B for control networking, the European EN14908 building-automation standard, and even IEEE 1473-L for in-train controls, have incorporated the LonWorks platform along with its physical-layer signaling over power-line and twisted-pair wiring.

Despite such successes, however, neither LonWorks nor any other home-networking technology has taken off in the market. There are several reasons for the faltering of home automation. One is that no one technology offers all of the attributes that consumers demand in their technology. Another is the lack of a killer application to jump-start widespread adoption with its inevitable cascade of decreasing costs, increasing public awareness, and competition-fostered innovation.

A technology must possess many attributes to be successful in a consumer market such as home automation. These features include:

- **Affordability**: The technology must provide enough benefits with a low enough price that consumers become willing to invest in it.
- **Ease of use**: The technology should be simple enough to install that the average consumer can use it out of the box.
- **Reliability**: Once consumers install it, the technology should work as they expect without interruption and without their attention.
- **Flexibility**: Consumers expect to use technology where and how they wish without significant restrictions.
- **Long operating life**: Consumers expect their investment to pay dividends over months or years without fail. In the case of battery-operated devices, long battery life is essential for consumer satisfaction.
- **Interoperability**: Consumers expect to be able to purchase technology components from a variety of competing sources and have the components work together without effort.
- **Capability**: Consumers have come to expect that a newly adopted technology will provide several important benefits and useful features and that the technology's capability and features will steadily increase over time.

AT A GLANCE

- After languishing for decades, home-automation networking appears ready to move into the mass market.
- Technology improvements in power-line and wireless signaling have lowered costs, boosted data rates, and increased reliability.
- Although many standards exist, no technology or implementation approach yet dominates.
- A killer application may be emerging in the form of energy-management initiatives.

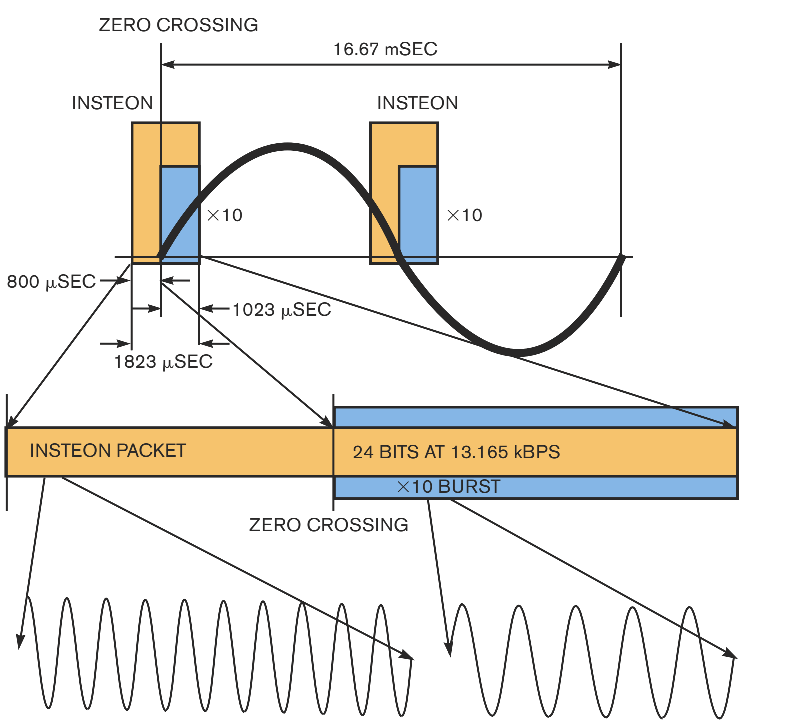


Figure 1 Insteon's power-line-signaling approach uses high-frequency bursts at the zero crossing to encode data bits, giving it a higher data rate than the older X10 technology, and it still retains interoperability (courtesy SmartLabs).

Currently, every available home-automation technology falls short in one or more of these areas, although proponents are continuously working to address these shortcomings. Sometimes, the shortfall arises purely from the communications medium. Home-automation systems use one or more of three media: wire and cable, power line, and wireless, typically RF. Each approach has its advantages and drawbacks.

Wire and cable media for home automation include twisted-pair wiring, coaxial cables, and optical fiber. These media have an advantage in their high data capacity and ability to provide a relatively noiseless communications channel for network signaling. Their major drawback is cost. Estimates for the installation of cable in construction range from $65 per linear foot for residences to nearly $300 per linear foot in industrial settings. Costs are lower when installation occurs during new construction but still remain too high for most consumers.

A second drawback of wire and cable media is inflexibility. Consumers are not free to relocate controls or endpoint equipment as they wish. The location of the installed cabling restricts placement, and the cost of new cabling is prohibitive.

POWER-LINE SIGNALING

In response to the drawbacks of cabling, home-automation technologies seek to use one type of wiring in every residence: the power line. As a networking medium, a power-line connection has two advantages. One is that they are

in place and run to nearly every location where endpoint devices exist. The second is that endpoint devices need no external power source, such as a battery. Both help satisfy the low-cost and ease-of-use requirements of a consumer technology.

Power-line networking has its challenges, however. The medium is noisy, carrying a variety of voltage spikes that arise as lights and motors switch on and off, loads change, and disturbances on the power grid propagate into the home. As a result of this noise, power-line-networking technologies have either restricted their signaling bandwidths or employed sophisticated and expensive noise- and error-reduction strategies.

The X10 standard serves as an example of the first approach: restricted bandwidth. To avoid noise, X10 signaling occurs during the zero crossing of ac power. A burst of 120 cycles at 120 kHz, repeated at the next zero crossing for basic noise immunity, signals a one, and its absence signals a zero. The result is a raw data rate of 60 bps, with synchronization, framing, and addressing bits adding overhead to reduce the achievable data rate by 60%. This low data rate prevents the network from handling any but the most basic control and sensing functions and adds considerable latency when implementing a string of commands.

The SmartLabs' Insteon offers a similar approach (**Figure 1**), transmitting a packet of 24 bits at the zero crossing, each bit encoded as 10 cycles of 131.65 kHz. It achieves a sustained bit rate of 2880 bps, greatly improving its utility and latency compared with X10. Yet, the similarity in technique allows Insteon networks to control X10 devices, providing a measure of the interoperability attribute that consumers demand.

A third variation, the Universal Powerline Bus, comes from Powerline Control Systems. This system imposes 40V-dc spikes on the power line at the zero crossing, using pulse-position modulation to encode 2 bits per zero crossing. Filtering prevents the spikes from generating excessive EMI on the power lines. The data rate is on the order of 100 bps.

These low data rates, however, limit what the network can achieve, thus failing to provide much of the capability attribute that consumers expect of technology. Yet, achieving higher data bandwidths using the power-line approach requires a more sophisticated signaling approach and protocol. Echelon's PL3120 power-line transceiver, for instance, includes a DSP-enhanced processor for data recovery and noise reduction, achieving a sustained data rate as high as 5.4 kbps.

Dramatically higher rates have become available over the last few years. The HomePlug Powerline Alliance's new HomePlug AV standard, using technology from Intellon, employs orthogonal-frequency-division multiplexing to generate signals that attain data rates as high as 200 Mbps. This speed is fast enough for the network to go beyond simple control of lights and power and serve as a communications channel for entertainment media, such as IPTV (Internet Protocol television). It remains

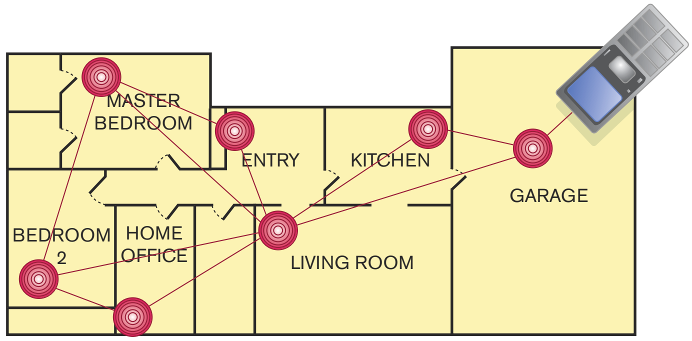


Figure 2 Enough nodes to provide multiple links in the mesh can handle the limited range of wireless signaling (courtesy Z-Wave Alliance).

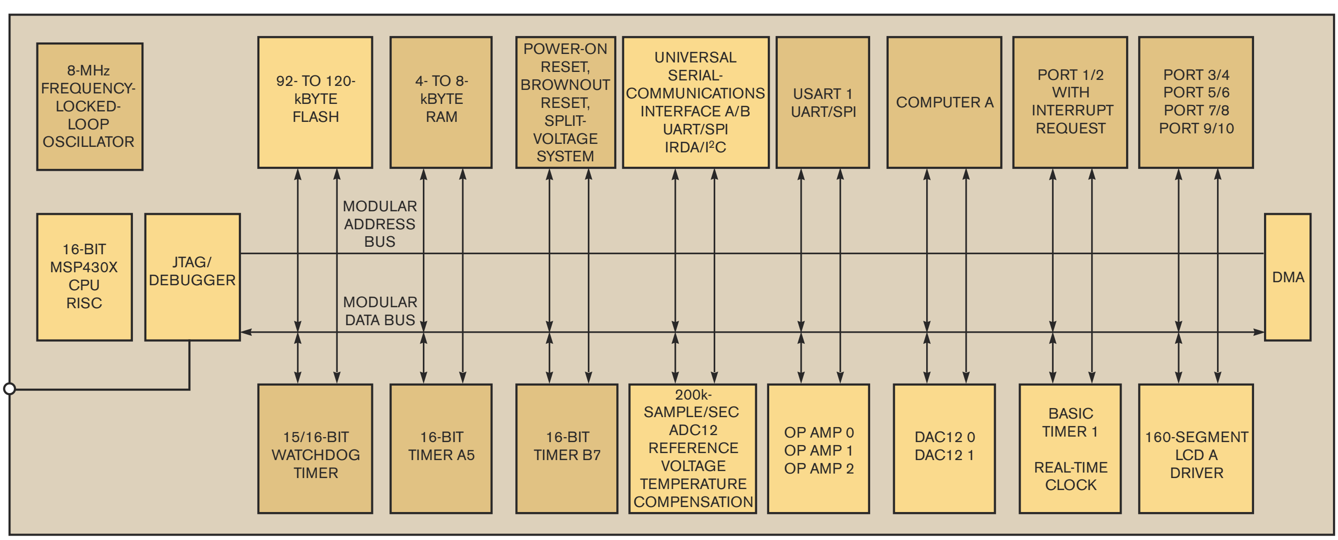


Figure 3 Making the peripheral functions of the microcontroller capable of acting without CPU supervision helps save power and extends the battery life of home-automation nodes (courtesy Texas Instruments).

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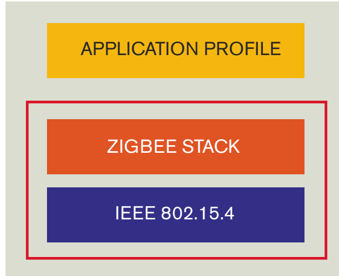


Figure 4 Compatibility may have many meanings in ZigBee devices, because the standard defines different levels for just the radio and the stack, for devices with custom application software, and for products conforming to a public-application profile (courtesy ZigBee Alliance).

to be proved, however, that the cost for this sophistication will drop to the levels needed for widespread adoption.

Power-line signaling also has other drawbacks that can impact its long-term success. In US homes, for instance, power comes to the house as two out-of-phase, 120V feeds with a neutral line. This arrangement allows the wiring of 240V power for demanding appliances, such as furnaces and dryers, and allows regular household power to run at the safer 120V level. The result, however, is that the power lines in the house split among the two phases, and power-line signaling cannot reliably cross between the phases without the help of either a bridge node or a high-frequency shunt between phases. This step adds complexity and cost that consumers may not tolerate to the implementation of a home network.

Power-line signaling also has a limitation to its installation flexibility: It requires that power lines be present at every node in the system. This situation imposes restrictions on the placement of control nodes, such as light switches and thermostats. Ideally, consumers would want to locate anything anywhere with no restrictions.

This level of flexibility is one of the main benefits of the wireless-RF medium. Several wireless-home-automation-network technologies have arisen, including Z-Wave and ZigBee. In addition, home-networking technologies such as Echelon's LonWorks, SmartLabs' Insteon, and the European KNX have adopted wireless signaling in addition to power line to gain the added flexibility.

Until recently, however, RF-based networking has faced significant reliability challenges. To avoid licensing issues, RF-based networks typically work in one of the open-frequency bands for products such as microwave ovens, portable phones, and the like. The Z-Wave approach, for instance, operates in the 900-MHz ISM (industrial/scientific/medical) bands, which differ between the United States and Europe. ZigBee also operates in this band but is concentrating future development in the 2.4-GHz spectrum, in which frequencies are usable worldwide, allowing design of universal radio devices. In either case, however, the presence of other users in the open bands has the potential of creating a severe interference problem.

Supporters of the RF approach have been addressing the issue of interference and now appear to have solved it. Reports from ZigBee Alliance members Ember, Freescale, Microchip, and Texas Instruments, for instance, all agree that the latest revision of the specification, ZigBee 2006, ensures robust operation even in the presence of in-band interference from other users, such as Wi-Fi. Components based on ZigBee 2006, which saw release in December, should soon be available to home-automation-product designers.

Software, too, can play a role in resolving interference issues and ensuring reliable network operation. Officials at ZigBee-application-software vendor Airbee Wireless note that the ZigBee-protocol implementation can impact the network's performance in a dirty RF environment. Airbee's software, for instance, includes network-management functions that allow measurement of signal strengths and can actively respond to interference sources through channel selection and message routing. Fixed routers can also use signal strength to triangulate and identify interference sources and alert the user.

Still, other issues exist. Supporters of the power-line approach point to the limited range of RF devices and their potential need for battery power as significant drawbacks of the RF approach. Because the RF-home-automation networks use self-configuring mesh architectures, however, their supporters claim that range is not an issue. Simply adding nodes with message-relay capability

in appropriate locations will ensure that everything connects (**Figure 2**).

Battery life is more of a concern to RF-home-networking suppliers. An RF-based home network can potentially contain several hundred nodes, many of which are battery-powered. Consumers do not want to change dozens of batteries every few months to keep their systems operating.

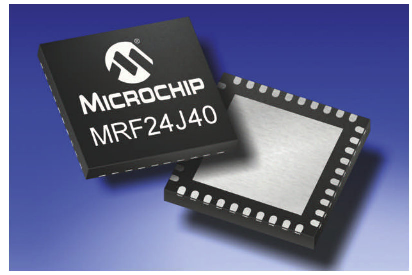
Several approaches for maximizing battery life now exist. The Z-Wave approach, for instance, allows nodes to remain inactive most of the time to conserve power. They wake when an event such as a button press requires a response and periodically to see whether any network traffic is addressed to them, remaining in a low-power state the rest of the time. ZigBee nodes offer a similar approach. The underlying IEEE 802.15.4 radio standard works at low duty cycles, transmitting energy only in bursts. In both cases, relay nodes need to remain continuously active to maintain links, but those nodes typically are not battery-powered.

The other new approach to battery

> INTERNATIONAL BODIES ARE ATTEMPTING TO CREATE WORLDWIDE STANDARDS TO TIE TOGETHER ALL THE MANY ASPECTS OF HOME NETWORKING.

life is the design of microcontrollers and other ICs for implementing home-networking nodes that have active power management. Vendors such as TI's Chipcon division have come up with microcontroller devices that minimize power consumption by keeping active only the functional blocks needed at any given time. Chipcon divides the MSP430FG461x family microcontrollers, for instance, into multiple functional blocks (**Figure 3**) that can carry out their tasks without involving the core processor. This situation minimizes power draw and allows nodes to operate on batteries for years without replacement.

Technological advances have thus brought a variety of home-networking



The availability of single-chip radios and microcontroller/radio combinations is lowering the cost of wireless home networking (courtesy Microchip Technology).

approaches to levels that will allow the dream of intelligent houses finally to become reality. Two roadblocks still remain, however. One is interoperability. Many companies base their approaches on proprietary technology, which limits the number of suppliers from which consumers can choose. The other roadblock is the lack of a compelling application to jump-start the market.

To solve interoperability issues, vendors of home-automation technologies have turned to standards and trade associations. Echelon's LonWorks technologies have the support of the Digital Home Alliance, providing a broad base of suppliers and certifying interoperability among devices. The Z-Wave Alliance provides a similar function for the Zensys Z-Wave technology. The HomePlug Powerline Alliance supports Intellon's HomePlug technology. Other industry groups include the UPnP (Universal Plug and Play) Forum and the ZigBee Alliance, both working to ensure interoperability and to refine their standards.

On a higher level, international bodies are attempting to create worldwide standards to tie together all the many aspects of home networking. The ISO/IEC JTC (International Standards Organization/International Electrotechnical Committee Joint Technical Committee) has formed the JTC1/SC25/WG (Working Group) 1 to define a set of standards creating a single network for all of a home's electrical and electronic devices. The scope of the proposed standards ranges from heating and air conditioning to appliances and home entertainment, with ties to home computers and the Internet. Work is still ongoing in this definition effort, although several standards have already seen release.

Developers should examine the lev-

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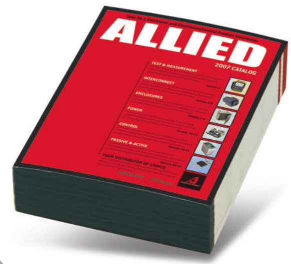

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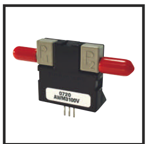

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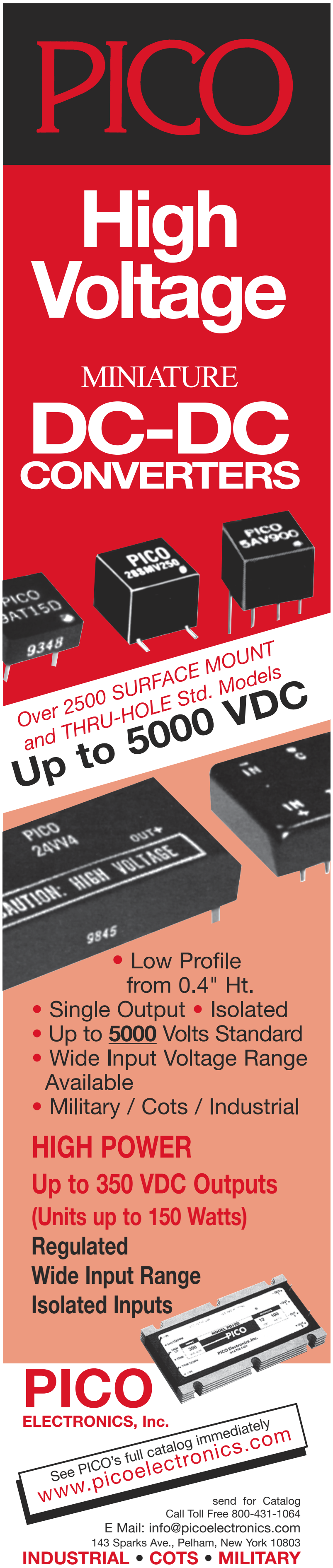

els of certification that standards call for and trade organizations provide, however, to ensure that they are appropriately targeting their designs. In the case of ZigBee, for example, several levels of compliance exist, and not all ensure interoperability in a home-networking application. The ZigBee protocol lies above the IEEE 802.15.4 radio standard, with application software sitting above the protocol stack (**Figure 4**). ZigBee Platform Certification ensures that the compliant device will interoperate in a network but says nothing about its application. Certification of a manufacturer-specific platform ensures that the device will not interfere with other ZigBee devices but does not ensure application-level interoperability. A device must achieve certification to a public profile for a given application, such as home networking, to guarantee the kind of interoperability that consumers demand.

Even with the ambiguities and competing standards, however, the field is now ready to begin delivering some of the wildest dreams of home-automation proponents. The range of media choices ensures that flexible and low-cost installation options are available. Data rates are high enough to allow distribution of entertainment and data as well as control over the networks. RF-signal-strength triangulation will allow systems to monitor and adapt to user locations, turning lights on before entering and off after leaving a room and switching music from room to room as the user moves. And developers are creating links to the Internet for remote operation of the systems as well as downloading media for many of the home-automation approaches in the market.

THE KILLER APP?

As exciting as these possibilities seem, however, from the consumer's viewpoint they represent just the gravy. Alone, they will not fuel the market. The meat of home automation, the killer application, must command widespread acceptance of the technology.

Such an application may be emerging. Power companies in both Southern California and Texas are looking to technologies such as ZigBee to help them implement load control and demand-based pricing in the home. With a ZigBee link from the meter into the home, these companies hope to provide

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customers with real-time feedback on energy use and cost as well as adjust user demand by remotely turning thermostats up or down, turning off water and pool heaters, and the like.

As energy costs continue to rise, such uses of home-automation technology can become compelling and may become mandatory. It's a humble beginning and less exciting than an intelligent home that conforms itself to your presence and preferences, but it may be all the home-automation industry needs to gain entry to the consumer's home. From there, the approaches that best satisfy the many requirements of consumer technology can see the kind of opportunity growth that the PC industry enjoyed in the late 20th century. **EDN**

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Contributing Technical Editor Richard A Quinnell has been covering technology for more than 15 years after an equally long career as an embedded-system-design engineer.

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BRIEF

TPS6108x: A Boost Converter with Extreme Versatility

By Jeff Falin
Senior Applications Engineer

Introduction

The TPS61080 and TPS61081 are highly integrated boost converters that have adjustable outputs of up to 27 V with input voltages as low as 2.5 V. The difference between the two versions is the current-limit rating of the integrated power switches (typically 0.5 A and 1.3 A, respectively). The TPS6108x boost converters adopt a traditional current-mode-control scheme and constant pulse-width-modulation (PWM) frequency for low-noise operation. The switching frequency can be configured to either 600 kHz for light-load efficiency or 1.2 MHz for smaller external components. With integrated feedback compensation, internal power switches, and fast PWM switching, the 3 x 3-mm QFN package enables an extremely small boost converter for a wide variety of applications. An example is a 12-V or 24-V industrial power rail from a 3.3-V or 5-V bus. Additional features include high efficiency, an adjustable reference voltage, and redundant protection circuits—all of which makes the TPS6108x ideal for boosting the 3.6-V Li-ion battery voltage used in most portable applications. The converters also support the higher voltages needed for powering TFT LCD displays, OLED displays, WLED backlights, or camera flashlights.

Powering Displays

Figure 1 shows the converter in a typical boost configuration that provides a regulated output voltage.

When up to 20 V and 100 mA per column are required to drive a passive-matrix OLED (PMOLED), the 1.3-A switch rating makes the TPS61081 the best choice. When providing less than 10 V and tens of milliamps per column for the active-matrix OLED (AMOLED), the 0.5-A switch rating of the TPS61080 may be appropriate. In either case, the low-$R_{DS(on)}$ internal switches and the choice of switching frequency provide optimal supply efficiency. Figure 2 shows efficiency data for a 12-V output when a Li-ion battery with a typical 3.6-V source voltage is used.

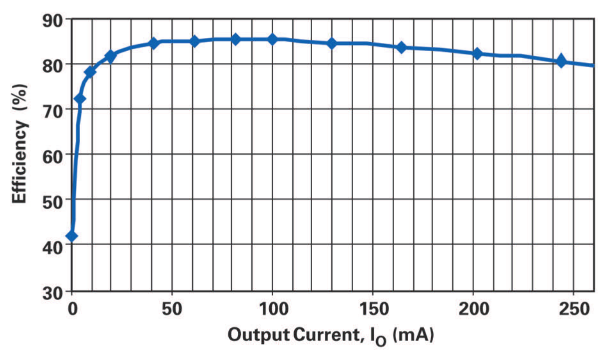

Figure 2. Efficiency with V_{IN} = 3.6 V

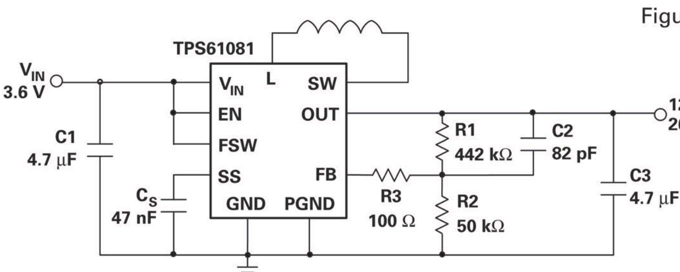

Figure 1. Typical application for a 12-V boosted output

To support the gates of the thin-film transistor drivers for active-matrix-LCD or OLED displays, the high-voltage rail must be capable of fast transients. The TPS61080 has current-mode control and optimized internal compensation; and it can operate at 1.2 MHz with a 4.7-µH inductor, making it ideal for fast-transient response. Figure 3 shows the transient response of the TPS61080, which was configured as shown in Figure 1 except for an additional 4.7-µF output capacitor.

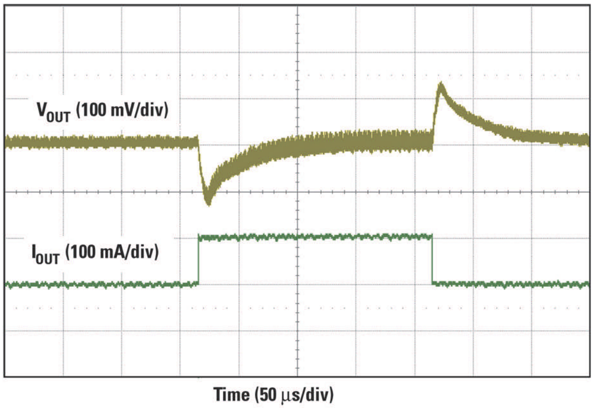

Figure 3. Transient response of TPS61080

WLED-Display Backlight Driver

As shown in Figure 4, most boost converters can be used to power WLEDs if the voltage feedback network is replaced with the WLED strings and a series current-sense resistor, R3. The TPS6108x can be used to drive several series WLEDs in parallel for backlighting larger displays.

The voltage across the current-sense resistor is fed back to provide regulation. Traditional boost converters use 1.2-V feedback voltages; therefore, the power loss due to R3 is $P_{LOST} = I_{WLED}^2 \times R3 = 1.2\,V \times I_{WLED}$. The TPS6108x converters have an SS pin that is used to provide variable soft startup for boosted voltage-regulation applications. The SS pin can also be used to lower the FB-pin reference voltage and to reduce sense-resistor power loss in a WLED current-regulation application. Simply connecting a resistor, R1, from the SS pin to GND will lower the FB-pin reference voltage. The reference voltage equates to the resistance of R1 times the SS-pin bias current (I_{SS} = 5 µA typical), resulting in the WLED current calculation:

$$I_{WLED} = \frac{I_{SS} \times R1}{R3}$$

A second resistor, R2, in series with the FET and Q1 and in parallel with R1 provides analog dimming by lowering the regulated FB-pin voltage across the sense resistor.

Protection

The TPS6108x also has pulse-by-pulse overcurrent limiting, which turns off the power switch once the inductor current reaches a preset value (0.7 A for the TPS61080 and 1.6 A for the TPS61081). The power switch turns back on at the beginning of the next switch cycle. When the inductor current stays above the short-circuit current limit for more than 13 µs or the V_{OUT}-pin voltage goes 1.4 V below V_{IN}, the IC assumes that there is a short-circuit condition and turns off the isolation FET. After 57 ms, the IC attempts to restart. If a momentary short is cleared, the output returns to its regulation voltage and switches normally. For a permanent short, the isolation FET turns off again and waits for power-on reset or EN-pin toggling. Although the isolation switch has a low $R_{DS(on)}$ for minimum power loss, shorting the V_{IN} and L pins can bypass the switch and further enhance the efficiency.

When the TPS61081 is configured for regulated current output as shown in Figure 4, the output voltage could run away if the output became high-impedance (i.e., if a WLED burned out or the load was disconnected). To prevent the power switch from exceeding its maximum voltage rating, the overvoltage-protection (OVP) circuit turns off the power switch when the output voltage exceeds the OVP threshold. When the output voltage falls below the OVP threshold, the converter resumes normal PWM operation.

Conclusion

This extremely versatile, integrated-FET boost converter is ideal for industrial, medical, telecom, and consumer applications that require boosted voltages. Features such as variable-reference voltage and the multiple-protection circuitry make the TPS6108x also well suited for powering LCD and OLED displays.

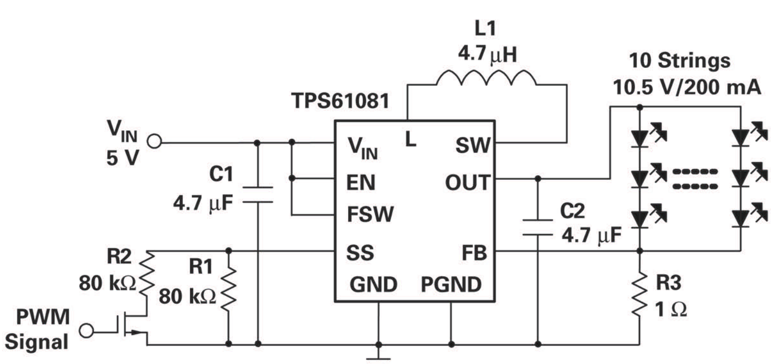

Figure 4. TPS61081 WLED backlight driver circuit

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1. TPS61080/1 Datasheet (SLVS644B)
2. *power.ti.com*

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Running an FPGA at ASIC speed

TAKE ADVANTAGE OF PROGRAMMABLE HARDWARE TO MAXIMIZE ASIC-PROTOTYPE SUCCESS.

The hardware-emulation team at Texas Instruments (www.ti.com) is getting word about its next project: developing a prototype of the modem of a baseband-processor ASIC for next-generation wireless handsets. The prototype is necessary to help the software team test its code using real hardware as soon as possible, because the processor itself won't be ready for another 12 to 14 months. Getting this head start on software development is key to the product schedule, because the software effort represents most of the overall engineering effort.

After hearing more details, the team leader knows he is in for a challenge. Testing the software requires an actual air interface, so the prototype needs to run at the same speed as the modem in the final ASIC. By itself, that part is not daunting; the team leader has lots of experience using FPGAs from several vendors to build prototypes that run at the same speed as the final ASICs. He estimates that the prototype will take multiple FPGAs to implement; even the smallest partition of the design that he would want to fit into a single device is larger than the largest FPGA available. Two other requirements, in combination with the performance requirement, present the team with its biggest challenges. First, the team must complete the prototype in little more than four months. Second, the RTL description of the ASIC is coming from another team, so the hardware-emulation team cannot change it, making partitioning and debugging difficult.

Thus began the emulation project for the modem of Texas Instruments' OMAPV2230 (Open Multimedia Applications Platform) digital-baseband and applications processor for advanced 3G handsets. Although the team had considerable experience developing multi-FPGA designs under deadline, the size of this design represented a new milestone for team members. This new ground, combined with extreme time pressure, forced the team to devise new strategies in addition to applying existing ones. Without knowing exactly how long it would take to complete certain portions of the project, the team focused on practices that would shorten task times and ease the overall development effort. What follows are some of the team's best practices and strategies for achieving that goal, which derive from its many projects, and examples from the OMAPV2230 modem project.

ASSESSING THE DESIGN

The project began with an assessment of the scope of the work. You'll need an estimate of your design size early on to make decisions about the size and number of FPGAs you'll need. You make this determination by counting pins, memory, and gates; in our experience, that is the typical order in which resources run out. Don't try to get perfect estimates of how many FPGA gates your design will require. It takes too long, and the risk of failure by underestimating the resource requirements can be catastrophic. Experience is the best way to get an estimate of how many FPGA gates your design will use. You can also get estimates of resource usage by function from FPGA and IP (intellectual-property) vendors; these estimates may vary widely, but it is better to err on the side of getting a worst-case estimate rather than a precise measurement.

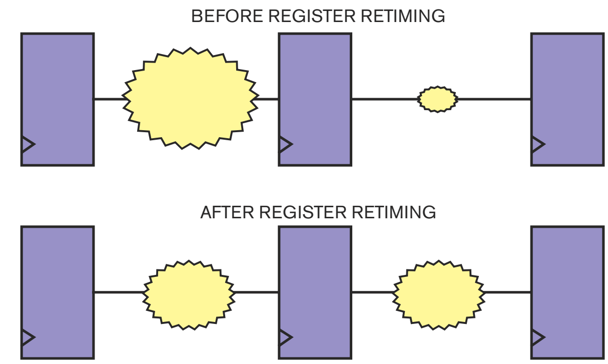

Figure 1 Pipelined, synchronous designs enable your design to benefit more from register retiming.

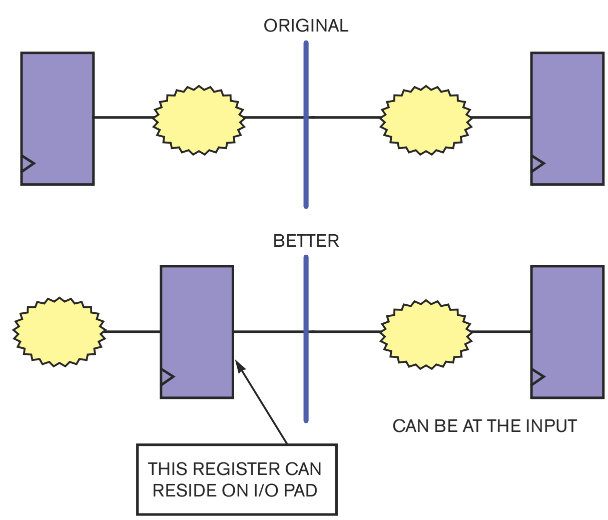

Figure 2 Registering your outputs results in more predictable delays and eases the burden of meeting timing constraints during compilation.

After you get an initial gate-count estimate, double it. By having more than enough FPGA resources on hand, you will ease and more than likely shorten your development effort. Design compilations that are not resource-constrained are generally a lot faster, and the amount of time you will probably save may help you avoid a lot of headaches. The emphasis here is to successfully prototype your design under time pressure, rather than save money on the cost of the programmable logic. Finally, you have a much better chance of extending the usefulness of your prototype platform if you have additional device resources available. (See **sidebar** "Postmortem" at the Web version of this article at www.edn.com/ms4233 for more information.)

BUILDING AND WRITING RTL

Try to split your design into smaller, unrelated problems for ease of tackling. Start problematic parts of your design, particularly bus interfaces, early. Design your system such that you can exercise and test individual blocks, even if they aren't yet present in the design. Besides helping out early in the development process when blocks might be available to test while you are still finalizing others, this practice also allows you to make progress when specific blocks of your design are under revision or otherwise unavailable.

Follow good synchronous-design practices; asynchronous designs that are possible in ASICs because of tight control over timing delays can easily run into trouble in FPGAs. Lots of pipelining, as well as registering all ports, also provides several benefits. First, it breaks combinatorial logic into more easily synthesizable portions. Pipelining also allows easier debugging, because FPGA-verification tools can easily access the inputs and outputs of registers. Finally, it allows more options for optimizing performance by register placement.

Figure 1 shows a pipeline of three registers in which a large amount of combinatorial logic is in place between the first two registers and relatively little combinatorial logic is in place between the second and the third register. By using a logic-synthesis option—register retiming—you can balance the amount of logic on either side, such that the worst-case combinatorial delays on both the input and the output sides of the registers are more equal. Register retiming is a relatively common logic-synthesis option and, in the case of this design flow, the team enabled it by simply turning on the option in the Altera (www.altera.com) Quartus II software's physical-synthesis settings.

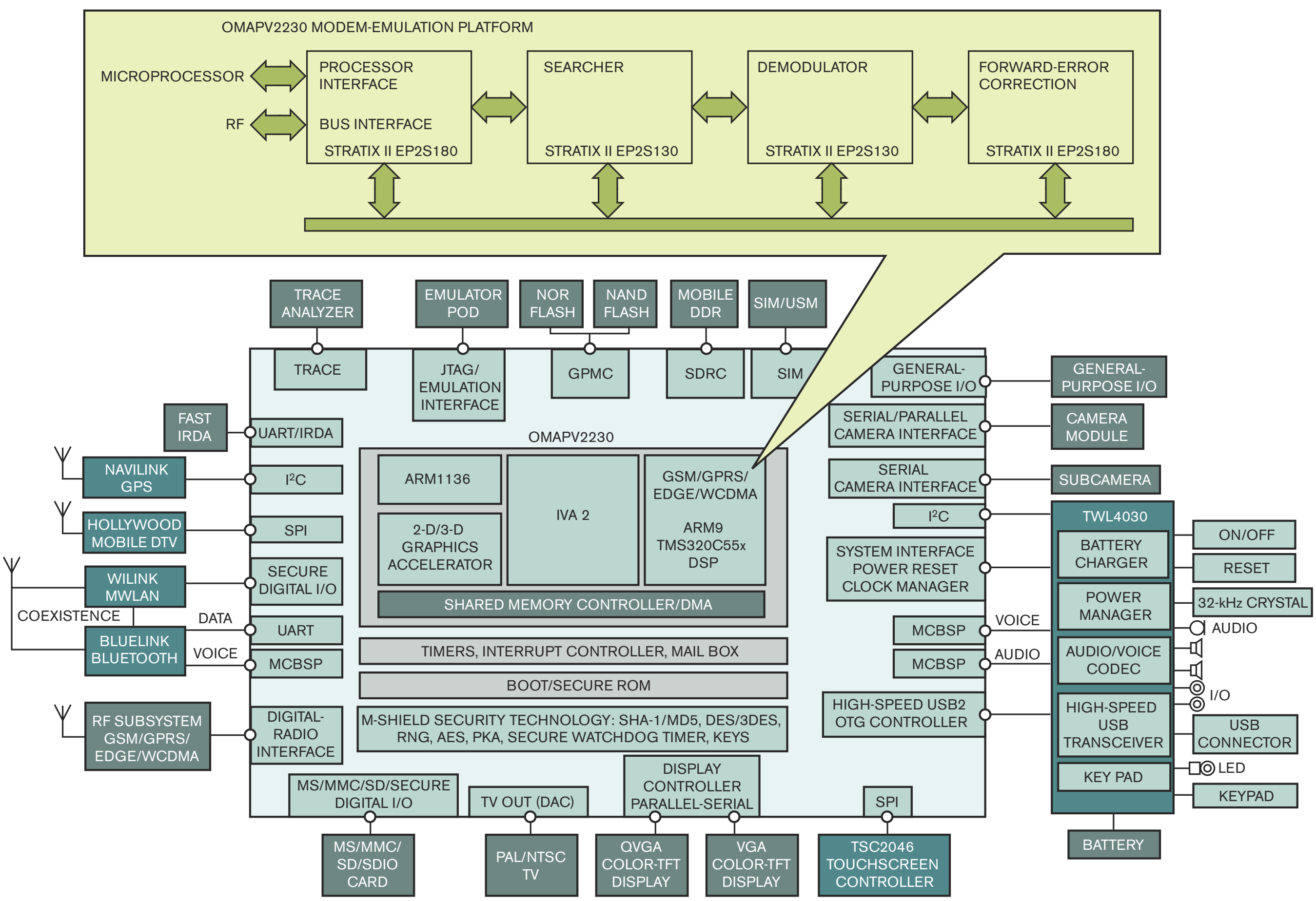

Figure 3 The OMAPV2230 modem-emulation platform partitions functions into Stratix II FPGAs.

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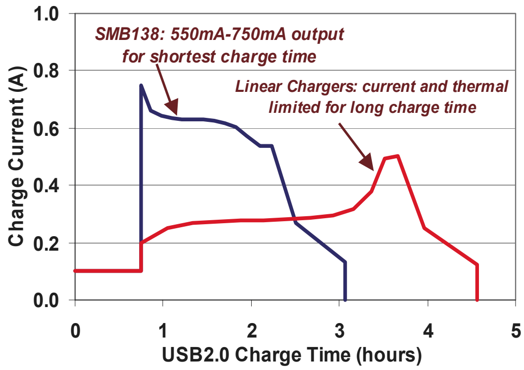

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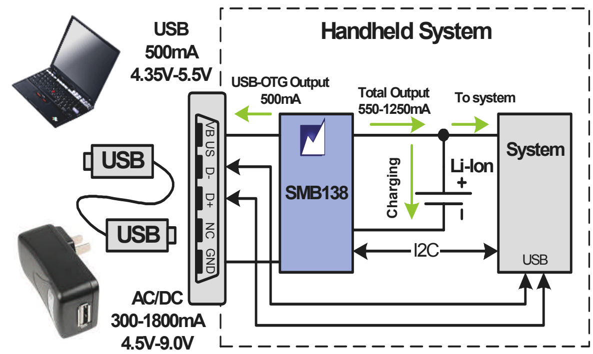

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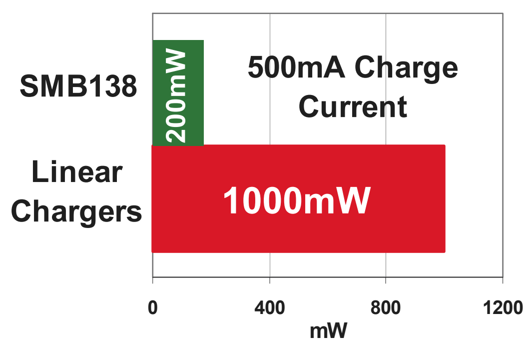

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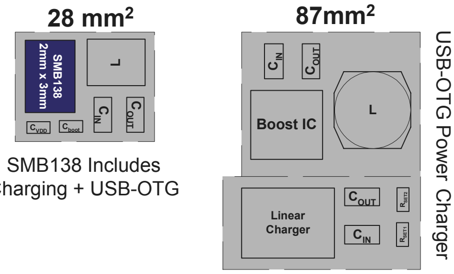

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Figure 2 shows the output of a register feeding logic to and from one FPGA and then feeding logic and a register into another FPGA. Moving the register to the edge of the device and placing it into an I/O element associated with the pin reduce the logic-synthesis burden and the associated compilation time. Doing so also results in a more predictable delay path from the output of the I/O register to the input of the register in the next device.

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If running your FPGA prototype at high speed is your goal, then it helps to code for the ASIC with the FPGA architecture in mind. On the other hand, if you have RTL code that mainly targets an ASIC, then you can get the best performance in your prototype by using FPGAs with a flexible logic building block, such as the Altera Stratix II devices that this project uses. In either case, using the same RTL database for both the ASIC and the FPGA design as much as possible helps minimize differences between the two. The OMAPV2230 project uses the same database with the exception of clocking and memories, which the team instantiated in wrappers.

One of the inevitable differences between the ASIC design and the FPGA design is memory, because the ASIC design includes memory structures that you must build from generic memory blocks in the FPGA design. A good approach to this situation is to code logical-level memories in your ASIC RTL, specifying the exact size you need, rather than using physical memories. The FPGA-synthesis tools can more efficiently map logical-level memories into the FPGA, providing better performance and resource usage. It is worth the extra level of hierarchy, even though you ultimately must map the memories into a physical memory for the ASIC. Also, it helps to standardize on positive- or negative-enabled memories within the ASIC RTL and then add inverters as necessary at the wrapper level. At the Web version of this article at www.edn.com/ms4233, the VHDL code in **Listing 1** illustrates the common practice of using physical memories in an ASIC-design description, and the VHDL in **Listing 2** shows how to change the physical memory to a logical-level memory, and it shows a separate wrapper for the ASIC design.

With an RTL that specifies logical-level memories, you can manually map the ASIC memories to the FPGA memories. The FPGA tools can make it easy to build and instantiate the memory structures you need. The OMAPV2230 project uses the memory megawizard in Quartus II software to aid this instantiation, which automatically generates a VHDL wrapper for the FPGA design. Using instantiated memories also provides the additional benefit of enabling the use of the Quartus II software's in-system memory-content-editing capability, which allows the user to capture and update the content of memories independently of the system clock—a valuable asset during debugging.

When mapping memories, it helps to have a variety of memory structures to choose from in the target FPGA. In the case of this modem design, which has lots of memories of approximately 1 kbit each as well as some larger ones, the portfolio of memory-block sizes that the TriMatrix memory architecture in Stratix II devices provides produced the most efficient mapping. You can also achieve a better mapping by taking advantage of the FPGA-memory features. For example, in one of the projects, the RTL includes bit-enabled memories. The memories in the target FPGA include hardware support for byte-enabled memories. After consulting with the ASIC team, we determined that byte-enabled memories would meet the need, and, by making this modification, we achieved a four-times-more-efficient mapping of the memory structures into the FPGA.

PARTITIONING THE FPGAs

Most of the team's prototyping projects require the entire FPGA design to run at the same speed as the ASIC, so the first consideration in partitioning designs is performance. The OMAPV2230 modem project required hardware-based verification to truly test the software with an actual RF interface and device. Using simulated data was impractical, because it was easier to use a real RF interface than try to generate all the data that would represent all of the cases we needed to test. To achieve a real RF interface, the prototype would need to run at the same speed as the modem in the final ASIC.

The next major considerations in partitioning the design are minimizing I/O connections between devices and monitoring memory usage in each device. These goals are often complementary to the performance goal, because minimizing on-chip/off-chip delays contributes to higher performance. You can do quick bottom-up compilations of your RTL blocks in the FPGA to get an idea of their logic and memory usage and I/O interactions. Automated partitioning tools are available to do this kind of work, and they are generally good at keeping statistics and running totals to do trade-offs. The team used no partitioning tools in the OMAPV2230 project for a couple of reasons. First, partitioning tools generally require that all the RTL in the project be available and synthesizable; with some projects, you may want to begin partitioning before the RTL is at this stage. Second, the team felt that the best quality of results would come from partitioning the design by hand with an understanding of the RTL, working first and foremost toward the performance goal. If the goal was not to get to speed, partitioning tools would have made the work easier.

You can also partition for ease of debugging. For example, if you are concerned about an interface, you can place it at the edge of a device with the interface feeding I/O pins, which makes it easy to monitor. In this case, the team partitioned the demodulator and forward-error correction into separate devices to get better visibility into their interaction and to enable the software team to access their interaction with a simple logic analyzer. **Figure 3** shows the modem-emulation platform, indicating the four Stratix II FPGAs and the role of the modem in the overall OMAPV2230 device.

Reserve some of your I/O pins for debugging if possible; the team's target was 20%. Many FPGA tools allow you to route internal signals out to spare I/O pins, and, in this case, the SignalProbe feature in Altera's Quartus II software served this need well, especially because of the limitation that the team not change the RTL. If you can't reserve these pins, don't worry; FPGA tools such as SignalTap allow you to monitor internal signals and bring them out through JTAG pins. SignalTap also played a significant role in extending the value of the platform.

Target FPGA usage should be 30 to 40%, which is not always

possible, especially in this case, in which the team is pushing the capacity of even the largest available device. In general, the closer you get, the easier it will be for you. This statement is not to say that you can't effectively use more or all of the FPGA resources; you certainly can. But designs that are not resource-constrained are easier for the FPGA-design software to handle and therefore faster to compile. For the amount of recompiling you'll be doing, you'll want to keep compilation times short; doing so can save lots of time in the long run, which is more valuable than saving some money on the cost of the FPGAs. Also, having lots of available resources makes it easier to get timing closure.

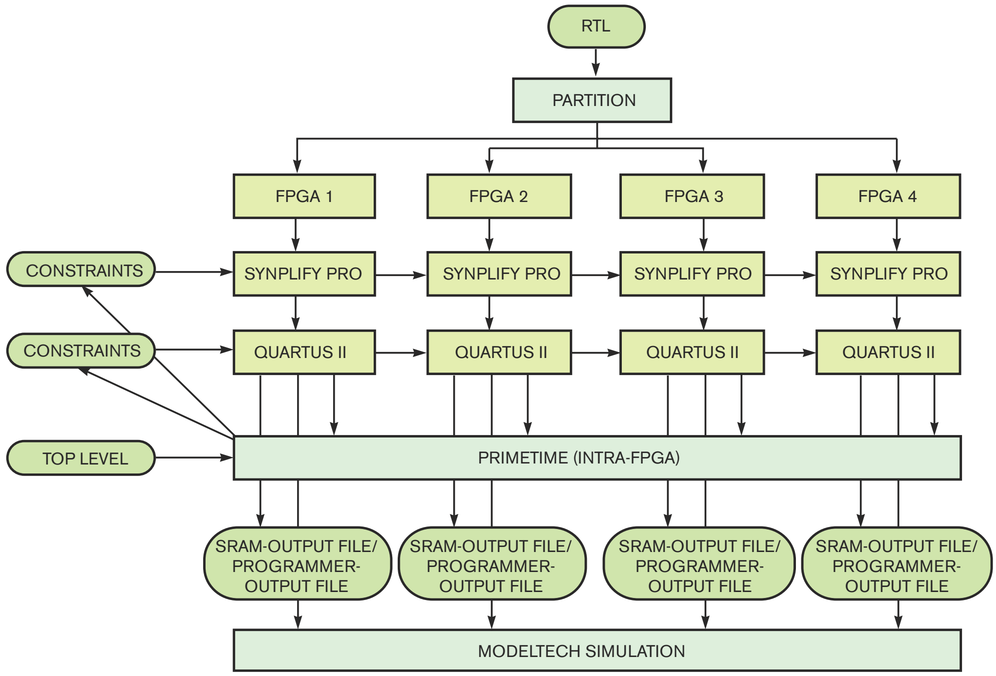

Figure 4 The TI hardware-emulation team relied on this tool flow to develop the OMAPV2230 emulation platform.

The OMAPV2230 project required devices with the most pins and logic resources, so the team chose Altera's Stratix II family to take advantage of the EP2S180 device. There was some risk in this decision because the EP2S180s were not available at the time the team started the project but were slated for release about three months later. A slip in that release date would have seriously jeopardized the project, but, in the meantime, the team had enough information and design support for the devices to make progress, including package pinouts to build boards and compilation support in the Quartus II software.

OVERENGINEERING THE BOARD

You can begin your board design as soon as you know which FPGAs and packages you will be using. Lay out board traces for as many of your FPGA I/O pins as possible. In this case, the team made board traces for every I/O pin and made generous use of Mictor connectors. Having the flexibility to probe every pin provides a great deal of debugging freedom.

Overestimate your power budget and put in a much larger power supply than you think you will need. You may find yourself clocking your FPGAs at higher than expected speeds or adding significant amounts of logic to your design in this or future projects and thereby drawing more power. The team found pin-compatible power supplies and initially chose ones that were larger than needed. In that way, the team had the option of using a smaller one when it came time to make many copies of the board.

For projects that require multiple FPGAs, use the same size and package device if possible. It's easier to remember one set of device characteristics, such as the amount of resources, features, clocks, and resets going to the same pins. Using the same devices also simplifies writing scripts and inventory control. If you have multiple teams working on the design, it's also a good idea to partition it such that no single FPGA overlays the domain of too many teams. This practice minimizes the impact that a single FPGA design has on the overall team and ideally enables most of the team to make progress even if one of the FPGA designs stalls.

RINSE AND REPEAT

Compiling an FPGA design for these kinds of projects often becomes an iterative process, as you try different tactics and design modifications to reach your performance target or as you focus on successfully completing one part of the design before moving on to another. It helps to develop a comprehensive script that you can run once to manage everything related to your FPGA flow, including choosing a synthesis option, applying compilation settings and performance constraints, extracting timing information, and performing timing analysis on your critical paths.

Compilation times for complex, multi-FPGA designs in the largest devices can take multiple hours and even longer as you place more performance constraints on them. During this time, you still want to make progress, so take steps to reduce compilation times and keep your team productive during these times. For example, eliminating false paths from your performance constraints helps minimize compilation times. With the latest timing-analysis tools from FPGA vendors, such as Altera's TimeQuest, it is now possible to specify multiple paths through multiple nodes and cut false paths from the analysis as easily as in ASIC-grade tools. Do not overconstrain your compilations; performance constraints increase compilation time, and exceeding your performance goal with your

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prototype doesn't necessarily provide any benefit.

Take advantage of both a dedicated synthesis tool and the FPGA software's native synthesis. The team used Synplicity's (www.synplicity.com) Synplify Pro as well as the synthesis that Quartus II software provides. You can use the best results from either, or one tool may provide a better description of a warning or error message than the other. In the case of the OMAPV2230, the team used multiple simultaneous compilations to explore paths toward meeting the performance goal of running at the same speed as the ASIC. The team used a dozen synthesis-software licenses on a server farm to perform compilations. Save all of your results and analyze them so you can make the best informed decisions on which actions to pursue. The team generated more than a terabyte of data and so had to enlist the IT group to support the amount of computer time and storage space it needed. **Figure 4** shows the FPGA-development flow, including synthesis, timing analysis, and simulation tools.

For simulation, the ideal situation is a single process for both the FPGA prototype and the ASIC design. To achieve this goal, you must develop the ASIC-simulation environment with the prototype in mind to support the gate-level netlists that the FPGA-design flow generates—for example, Mentor Graphics' (www.mentor.com) Modelsim. The team found that simulating the FPGA design is most valuable in the early stages of the project, in particular when debugging interfaces and drivers. As the FPGA design matured, the team relied less on simulation in favor of using the actual hardware platform. In the case of the OMAPV2230, the team simulated by using a testbench with the gate-level netlist that the FPGA-design flow generated and a top-level netlist to connect the multiple FPGAs. However, because of the long runtime, the team used this method for only the most elementary tests. In the end, the team relied on the hardware to provide the best verification; the team tested the design with the same interface and the same test equipment as the final ASIC. EDN

AUTHORS' BIOGRAPHIES

Edwin C Park is a staff engineer and member of the group technical staff at Texas Instruments, where he is responsible for advanced prototyping and architecture of 3G modems. He holds master's and bachelor's degrees in electrical engineering and a bachelor's degree in economics from Rice University (Houston). He enjoys gardening and hiking.

Martin S Won is a senior member of the technical staff at Altera Corp with more than 16 years of experience with programmable logic and programmable-logic applications. He joined Altera in August 1990 as an applications engineer and has held various positions in his career, during which he founded Altera's customer-training program and managed several other technical and marketing programs. His articles have appeared in many industry publications. Won holds a bachelor's degree in electrical engineering from the University of California—Santa Barbara, and his personal interests include reading, writing, hiking, and volleyball.

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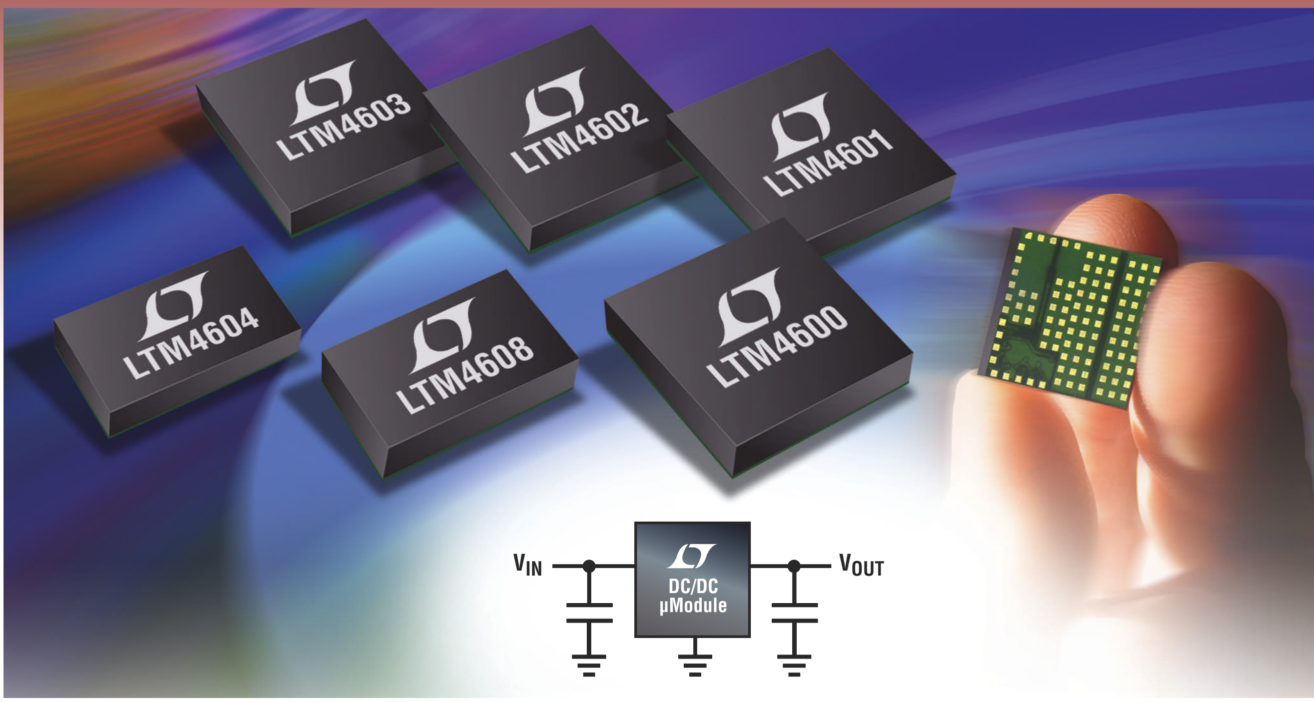

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New DC/DC µModule Family

V_{IN}: 4.5V-28V; V_{OUT}: 0.6V-5V						LGA Package	
Part No.	I_{OUT} (DC)	Current Share	PLL	Track, Margin	Remote Differential Sense	Height	Area
LTM®4602	6A	Combine two for 12A to 24A or 4x LTM4601 for ≤48A				2.8mm	15x15mm
LTM4603	6A		✔	✔	✔		
LTM4603-1	6A		✔	✔			
LTM4600	10A						
LTM4601	12A		✔	✔	✔		
V_{IN}: 2.5V-5.5V; V_{OUT}: 0.8V-3.3V							
LTM4604	4A	4x for 16A-32A	✔	✔		2.3mm	15x9mm
LTM4608*	8A		✔	✔	✔	2.8mm	15x9mm

*Future Product

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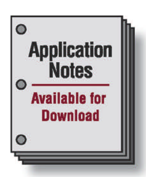
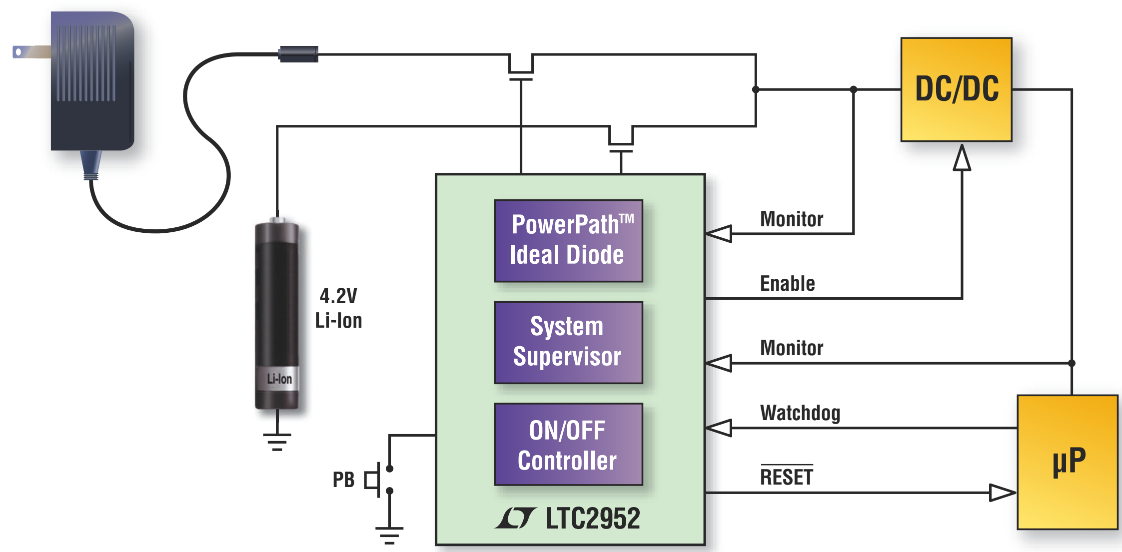


LINEAR TECHNOLOGY

Simplify PowerPath ON/OFF Control



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The LTC®2952 is a versatile power management IC with push button ON/OFF control of system power and system monitoring features. The power management function includes two power path controllers for applications requiring an ideal diode-OR function. The push button controller provides enable control for DC/DC converters, processor interrupt logic and adjustable ON and OFF debounce times. Robust supervisory functions make the LTC2952 an ideal fit in high reliability applications. Power-fail and watchdog reset functions provide further enhancements to ensure system integrity.

Features

Part No.	Supply Voltage (V)	Supply Current	ON Timer	OFF Timer	Kill Timer	Comments	Package
LTC2950	2.7 to 26	6μA	Adj	Adj	1024ms	Active high enable output (LTC2950-1), active low enable output (LTC2950-2)	TSOT-8, DFN-8
LTC2951	2.7 to 26	6μA	128ms	Adj	Adj	Active high enable output (LTC2951-1), active low enable output (LTC2951-2)	TSOT-8, DFN-8
LTC2952	2.7 to 28	25μA	Adj	Adj	Extendable	Push button power path controller with system monitoring	TSSOP-20, QFN-20
LTC2954	2.7 to 26	6μA	Adj	Adj		Interrupt logic for menu driven applications. Active high enable output (LTC2954-1), active low enable output (LTC2954-2)	TSOT-8, DFN-8

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AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Build a complete industrial-ADC interface using a microcontroller and a sigma-delta modulator

Patrick Weber and Craig Windish,
Siemens Energy and Automation, Pittsburgh, PA

DIs Inside

Designers commonly use 0- to 20-mA, 0 to 10V isolated inputs for industrial-application-control signals. A combination of isolated supplies, the built-in isolation of an Analog Devices (www.analog.com) AD7400 sigma-delta modulator, and a Texas Instruments (www.ti.com) MSP430 microcontroller creates a design for industrial designers requiring complete, isolated, and robust analog-signal interfaces. A precise signal-conditioning circuit generates the small differential voltage that the AD7400 requires (**Figure 1**). The circuit generates the required 200-mV differential voltage. For clarity, the **figure** omits overvoltage diodes and protection circuits.

A 0- to 20-mA current loop converts to a voltage through a properly scaled resistor, R_2, and enters a precision operational amplifier. The signal level, which connects to the negative input, gets a positive offset by maintaining constant voltage on the positive input of the amplifier. The 0 to 10V signal, such as that from a potentiometer, also scales to a similar voltage to that of the 0- to 20-mA sig-

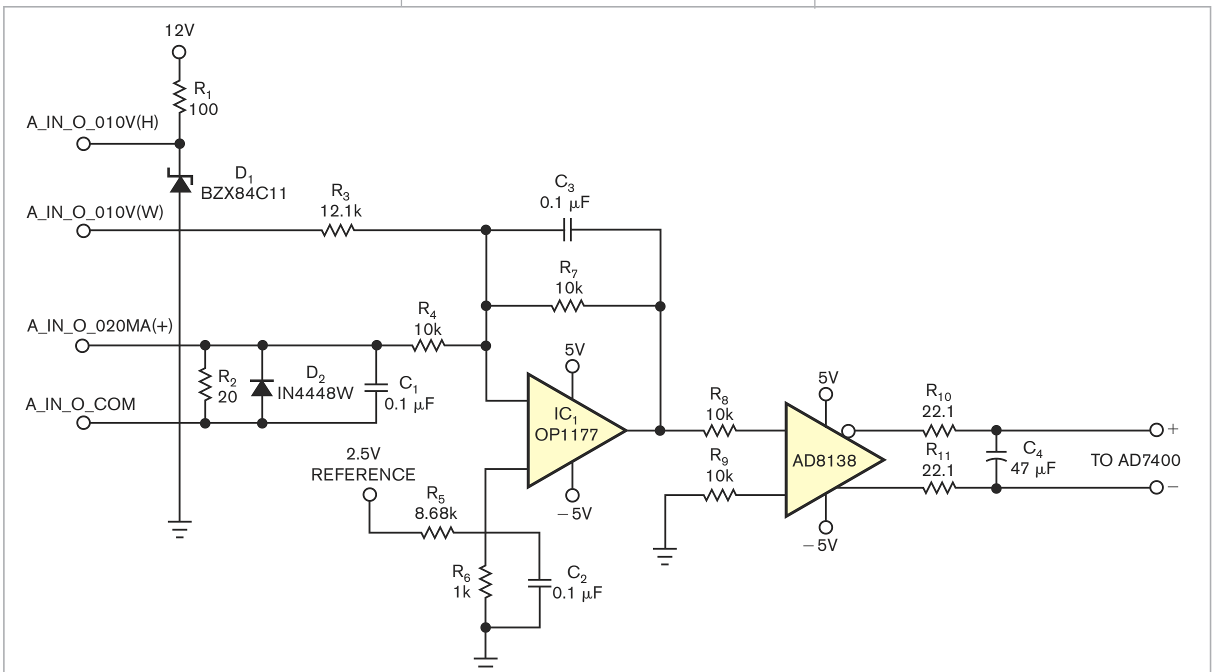


Figure 1 This analog-conditioning circuit filters and level-shifts the input signals, developing the AD7400 ADC's differential input.

nal and gets summed into the negative terminal of the Analog Devices OP1177 amplifier, IC_1.

Shifting the signal above 0V results in a signal that is similar to a positive, single-ended analog signal. A differential ADC-driver amplifier, Analog Devices' AD8138, drives the AD7400. The gain scales such that the resultant signal is within ±200 mV, which the ADC requires. Finally, before connecting to the AD7400, the signal runs through a lowpass filter, which R_{10}, R_{11}, and C_4 create between the positive and the negative terminals. The AD7400 converts this differential signal and processes it using a low-cost microcontroller. Sigma-delta-modulator ADCs, such as the AD7400, commonly interface to an FPGA or a DSP. However, this approach comes at a high price in both cost and complexity. For cost-sensitive applications not requiring advanced filtering, you can use a simple microcontroller.

The AD7400 device has two outputs, MCLKOUT and MDAT (**Figure 2**). MCLKOUT, a 10-MHz clock, synchronizes the modulated data stream, MDAT. The AD7400 interprets MDAT as a percentage of ones over time. Because MDAT changes

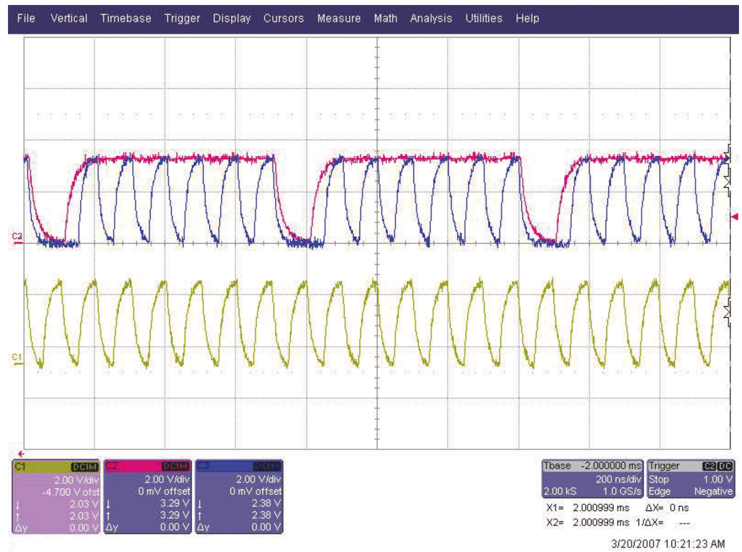


Figure 2 These oscilloscope traces show MDAT, inverted MCLKOUT, and the resulting data stream (courtesy LeCroy).

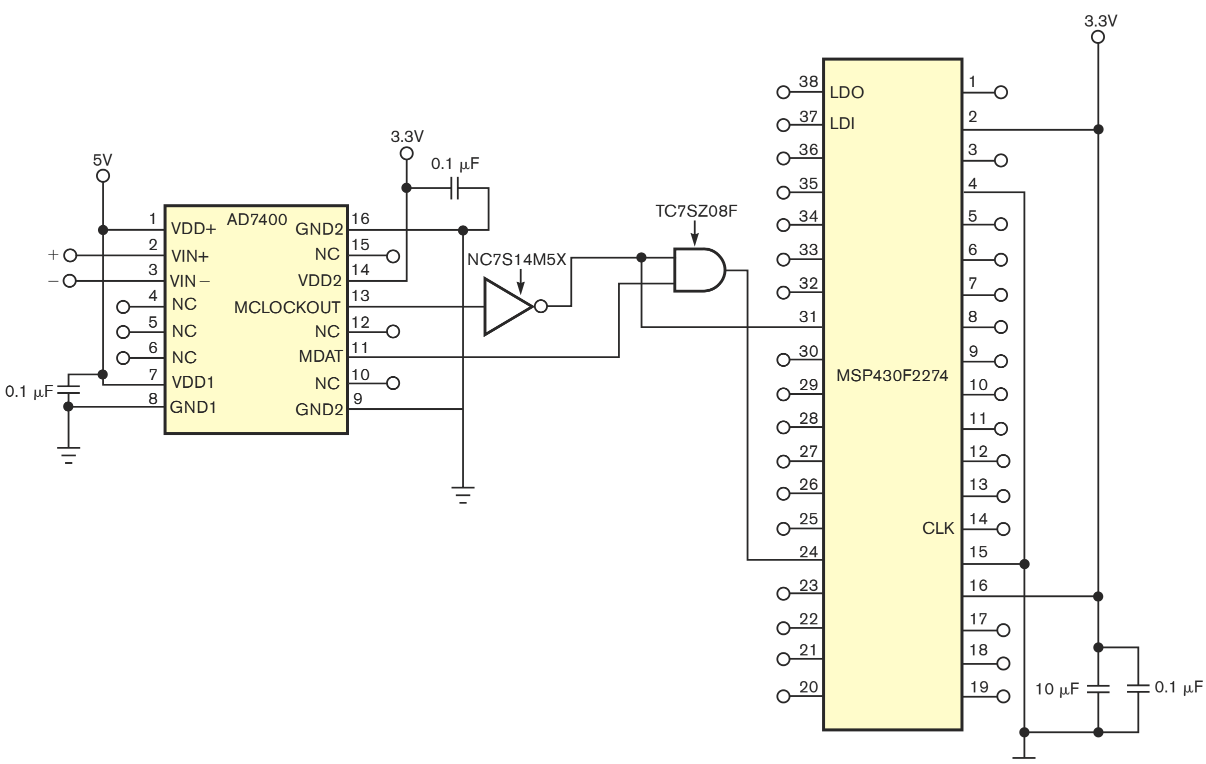
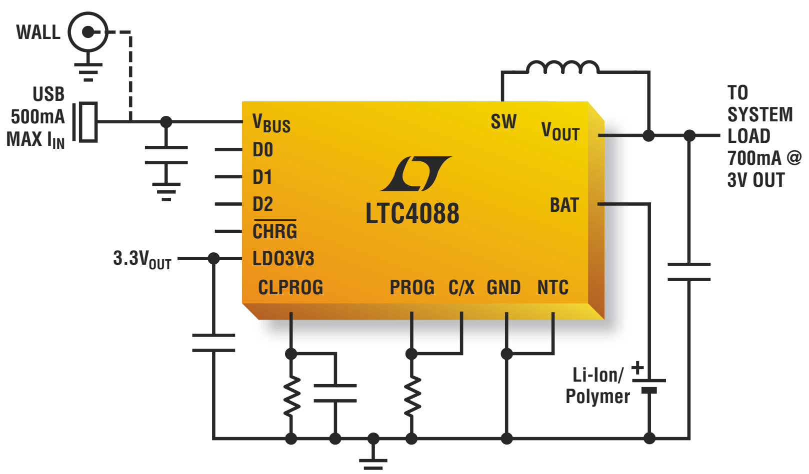
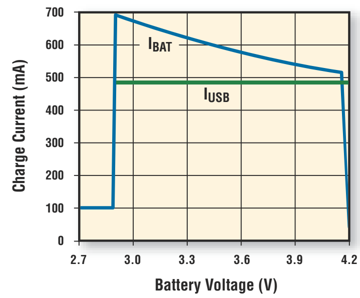
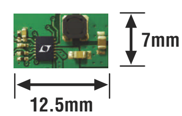


Figure 3 The AD7400 serial ADC digitizes the analog input and feeds the simple, low-cost microcontroller.

Get 700mA from Your USB Port







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High Efficiency, 1.5A Switching Battery Charger with PowerPath™ Management

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Li-Ion/Polymer PowerPath Managers

Part No.	PowerPath Topology	Input Voltage	Onboard Charge Termination	Package	Comments
LTC®4088	Switching	4.35 to 5.5V (7V max)	Timer with C/x Indication	3mm x 4mm DFN-14	Bat-Track™, Programmable Input I_{LIM} Maximizes Available Power from USB Port
LTC4066	Linear	4.35 to 5.5V (7V max)	Timer with C/x Indication	4mm x 4mm QFN-24	Integrated 50mΩ Low Loss Ideal Diode
LTC4085	Linear	4.35 to 5.5V (7V max)	Timer with C/10 Indication	3mm x 4mm DFN-14	Integrated 200mΩ Low Loss Ideal Diode (<50mΩ Capable Option)
LTC4089	Linear	4.35 to 36V (40V max)	Timer with C/10 Indication	3mm x 6mm DFN-22	Bat-Track, "Instant-ON" Operation, High Voltage Input Switching, with Current Limiting from USB
LTC4067	Linear	4.25 to 5.5V (13V OVP)	Timer with C/10 Indication	3mm x 4mm DFN-12	Up to 1.25A Charge Current, Integrated 200mΩ Low Loss Ideal Diode
LTC4090	Linear	4.35 to 36V (60V max)	Timer with C/10 Indication	3mm x 6mm DFN-22	Bat-Track, "Instant-ON" Operation, High Voltage Input Switching, with Current Limiting from USB

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only at the rising edge of MCLKOUT, the circuit must AND together MDAT and MCLKOUT to create a stream of pulses that the microcontroller can count. The microcontroller first inverts MCLKOUT to prevent unintentional glitches from being counted at the transition edges of MDAT. The **figure** shows MDAT, inverted MCLKOUT, and the resulting data stream.

The pulsed data signal and the inverted MCLKOUT each feed into a separate timer/counter on the microcontroller (**Figure 3**). The TI MSP430F2274 provides two 16-bit counters and can support operation as fast as 16 MHz. The circuit measures the ADC value by sampling the data counter when the clock counter signals an overflow interrupt. For this application, running an average number of data measurements on a circular buffer may conveniently filter the data.**EDN**

Circuit guards amplifier outputs against overvoltage

John Guy, Maxim Integrated Products, Sunnyvale, CA

A universal requirement for automotive electronics is that any device with direct connections to the wiring harness must be able to withstand shorts to the battery voltage. Though brutal, this requirement is necessary for reliability and for safety. One example of the need for this protection is an audio amplifier that produces indicator noises in the automotive interior. Though operating from a voltage of 3.3 or 5V, which is lower than the battery voltage, the amplifier must be able to stand off the full battery voltage. You can also use a protection network appropriate for these amplifiers for other automotive circuits (**Figure 1**). A dual N-channel MOSFET disconnects the amplifier's outputs from the wiring harness in response to a high-voltage condition on either output. The MOSFETs, Q_{1A} and Q_{1B}, are normally on; zener diode D_4 and its bias components drive the MOSFETs' gates to approximately 11V. Dual diode D_3 provides a diode-OR connection to the dc voltage on each output, thereby producing a voltage that controls the output of shunt regulator IC_2. The circuitry protects IC_1, a 1.4W Class AB amplifier suitable for audible warnings and indications for the automotive electronics.

During normal operation, the amplifier outputs' dc components are at

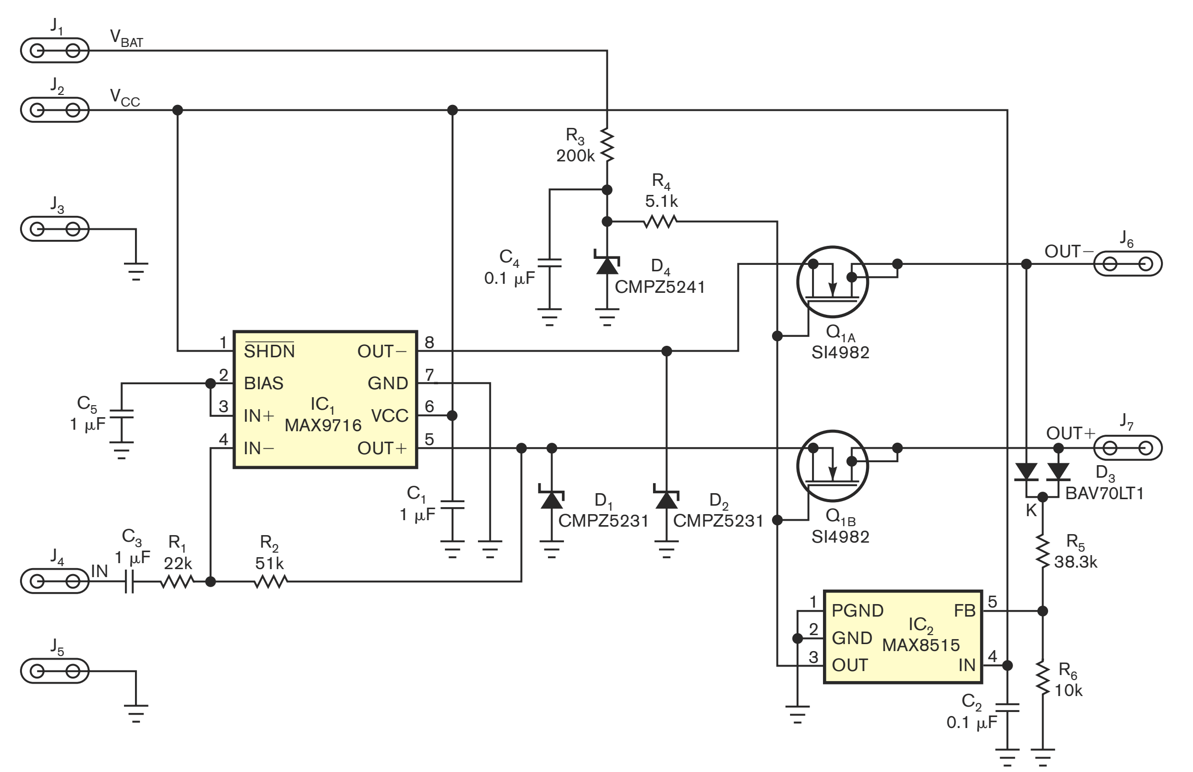

Figure 1 This output-protection circuit provides continuous protection against overvoltage faults.

DESIGN NOTES

One IC Generates Three Sub-2V Power Rails from a Li-Ion Cell

Design Note 419

Frank Lee

Introduction

Shrinking geometries in IC technology have pushed the operating voltages of today's electronics well below 2V, presenting a number of design challenges. One common problem is the need for multiple supply voltages: for example, one voltage for a CPU core, another for I/O and still others for peripherals. Sensitive RF, audio and analog circuitry may require additional dedicated quiet supplies, separate from less noise-sensitive digital circuits. As the number of supplies increases, it becomes impractical to use a separate power supply IC for each voltage and special-requirements subsystem. Board area would be quickly consumed by power supplies. One solution to the space crunch is power supply integration, provided by a triple regulator like the LTC®3446—three voltages from a single IC.

Triple Supply in a Tiny Package

The LTC3446 combines a 1A synchronous buck regulator with two 300mA very low dropout (VLDO™) linear regulators to provide up to three stepped-down output voltages from a single input voltage, all in a tiny 3mm × 4mm DFN. The 2.7V to 5.5V input voltage range is ideally suited for Li-Ion/Polymer battery-powered applications, and for powering low voltage logic from 5V or 3.3V rails. The output voltage range extends down to 0.4V for the VLDO regulators and 0.8V for the buck converter.

Each output is independently enabled or shut down via its own enable pin. When all outputs are shut down, V_{IN} quiescent current drops to 1µA or less, conserving battery power. The regulation voltage for each output is programmed by external resistor dividers. The buck regulator loop response can be tailored to the load by adjusting the RC network at the I_{TH} pin.

High Efficiency and Low Noise

The 1A synchronous buck provides the main output with high efficiency, up to 90%. This buck converter features constant-frequency current-mode operation at 2.25MHz, allowing small capacitors and inductor to be used. The two 300mA VLDO regulators can be connected to run off the buck output to provide two additional lower voltage outputs. This way, the buck performs the bulk of the step-down at the high efficiencies typical of switching

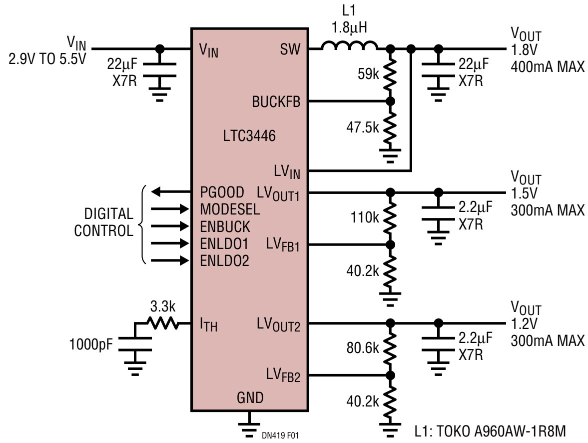

Figure 1. Schematic Showing the LTC3446 Power Supply Configured to Deliver 1.8V from the 1A Buck, and 1.5V and 1.2V from the 300mA VLDO Regulators. The VLDO Regulators Are Powered from the Buck Output via the LV_{IN} Pin.

regulators, while the VLDO regulators provide additional lower voltages with good efficiency at the extremely low noise levels typical of linear regulators.

The schematic in Figure 1 shows the LTC3446 configured to deliver 1.8V from the buck, 1.5V from the first VLDO regulator, and 1.2V from the second VLDO regulator. Figure 2 shows the Figure 1 circuit assembled onto a printed-circuit board.

Selectable Burst Mode® Operation or Pulse-Skipping at Light Load

The LTC3446's buck regulator features Burst Mode operation for optimum efficiency when operating at light loads, at the cost of increased output ripple and the introduction of switching noise below the 2.25MHz clock frequency. Burst Mode operation can be defeated by bringing the MODESEL pin high, which commands the LTC3446 to continue to switch at the 2.25MHz clock frequency down to very light loads, whereupon pulses are skipped as needed to maintain regulation. Figure 3, which shows the efficiency of the buck regulator vs load current, also illustrates the typical efficiency gains from using Burst Mode operation at load currents below 100mA.

Very Low Dropout (VLDO) Linear Regulators

The VLDOs in the LTC3446 employ an NMOS source-follower architecture to overcome the traditional tradeoff between dropout voltage, quiescent current and load transient response inherent in most PMOS- and PNP-based LDO regulator architectures. The V_{IN} pin (refer to Figure 1), supplies only the micropower bias needed by the VLDO control and reference circuits, typically at single-cell Li-Ion voltages. The actual load current is sourced from the LV_{IN} pin, which can be connected to the buck regulator output.

Each VLDO regulator provides a high accuracy output that is capable of supplying 300mA of output current with a typical dropout voltage of only 70mV from LV_{IN} to LV_{OUT}. V_{IN} should exceed the LV_{OUT} regulation point by 1.4V to provide sufficient gate drive to the internal NMOS pass device. Typical single-cell Li-Ion operating voltages extend down to 3.2V, supporting VLDO output voltages of up to 1.8V.

A single ceramic capacitor between 1µF and 2.2µF is all that is required for output bypassing. A low reference voltage of 400mV allows the VLDO regulators to be programmed to much lower voltages than are commonly available in LDO regulators.

Power Good Detection

The LTC3446 includes a built-in supply monitor. The PGOOD open-drain output pin is pulled low while any enabled output is more than ±8% from its regulation value. Once all enabled outputs are within this tolerance window, the PGOOD pin becomes high impedance. A microprocessor can monitor this open drain output pin to assess when a recently enabled output has completed startup.

Conclusion

The LTC3446 packs an efficient 1A buck regulator and two 300mA VLDO regulators in a tiny 3mm × 4mm DFN package. With an output voltage range extending down to 0.4V for the VLDO regulators and 0.8V for the buck, and an input voltage range covering the single-cell Li-Ion range up to 5.5V, the LTC3446 is ideal for powering today's multi-voltage, sub-2V systems.

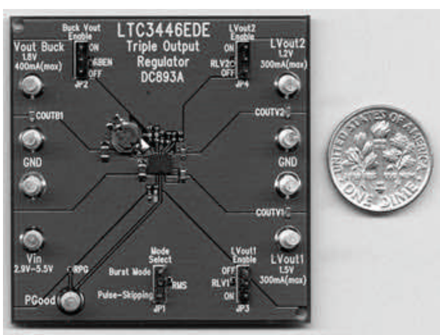

Figure 2. The LTC3446 Triple Power Supply Assembled on a Printed Circuit Board

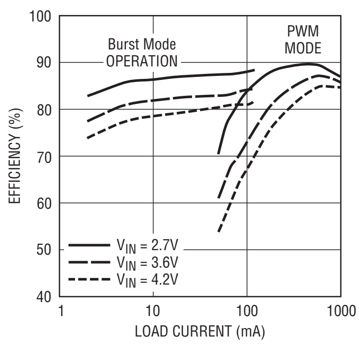

Figure 3. Efficiency of the LTC3446's Buck Regulator vs Load

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one-half of the V_{CC} supply—2.5V in this case, for which V_{CC} is 5V. The 11V gate drive fully enhances the MOSFETs, and the shunt-regulator output is off because its feedback input, Pin 5, is below its internal 0.6V threshold. If either output exceeds 5V, current flows through D_3 into the R_5/R_6 divider, pulling the feedback terminal above its threshold. The shunt-regulator output then pulls the MOSFET-gate voltage from 11V almost to ground, which blocks high voltage from the amplifier by turning off the MOSFETs. The MOSFETs easily withstand the continuous output voltage, and the circuit returns to normal operation when you remove the short. Because the circuit does not respond instantaneously, zener diodes D_1 and D_2 provide protection at the beginning of a fault condition.

The waveforms of **Figure 2** represent an operating circuit. One of the amplifier's outputs (Trace 1) is a 1-kHz sine wave biased at a dc voltage of 2.5V. Trace 2 is the signal on the wire harness. It also starts as a 1-kHz sine wave biased at a 2.5V-dc voltage, but, at 200 µsec, it shorts to an 18V supply. Trace 3 is the shunt regulator's output, initially biased at 11V but pulled to ground in response to the overvoltage condition. Trace 4 is current in the wire harness. Initially a sine wave, this current drops to zero in response to the overvoltage condition.

The components in **Figure 1** optimize this circuit for 5V operation. For other voltages, you can adjust the R_5/R_6 resistor values. The shunt regulator must be able to function in saturation and, therefore, requires a separate supply pin in addition to the shunt output pin. The circuit repeatedly withstands 28V shorts without damage. EDN

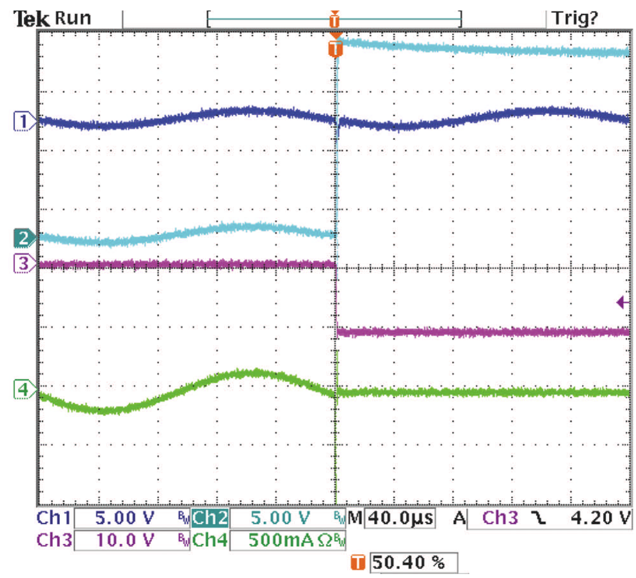

Figure 2 In Figure 1, one of IC_1's two audio outputs (Trace 1) has protection when its external terminal accidentally contacts an 18V supply voltage (Trace 2).

Isolated circuit monitors ac line

David Williams, Millington, MI

The circuit in **Figure 1** provides a low-cost, isolated ac-line monitor that measures ac-line-voltage level and has some other unique capabilities. The analysis of the circuit is straightforward: When the ac input, V_{IN}, is positive relative to neutral, you apply it to the network comprising R_1, R_2, D_1, and the LED in optocoupler IC_1. Current flows in this network when the voltage is high enough to get zener diode D_1 and the diode in the optocoupler to conduct. This diode pair's conducting voltage is the enable voltage, V_E. The zener diode's reverse-breakdown voltage of 47V and the optocoupler's LED forward voltage of 1.2V make the enable voltage 48.2V. Any voltage below this level drives the output of the optocoupler high. When the voltage exceeds the enable voltage, the transistor in the optocoupler becomes saturated, pulling the output low. The output continues to stay low until the input voltage drops below the enable voltage.

The resulting output is a square wave with a fixed time, t_{TOTAL}, based on how long the input voltage is above the enable voltage. If the voltage on the input varies from 120 to 144V, the resulting square-wave waveform becomes wider; if the voltage varies downward, the pulse width decreases. To calculate the formula for this circuit, consider the input waveform as a cosine function. Because the input voltage peaks at time zero, the optocoupler circuit is on, and the output voltage is low. It continues to be low until the input voltage moves below the enable voltage. The following **equation** yields the time when this crossover happens:

$$V_E=V_{IN}\times\cos(2\times\pi\times f\times t_{ON}).$$

Because the cosine function is symmetrical around zero, time t_{ON} is half the total time that the output pulse is high. Because a microprocessor's timer port usually captures the time, the simplest way to calculate the input voltage from the pulse width is to replace the on-time with the total time and then to solve the equation for the input voltage, which gives the result as a function of the measured pulse-width output from the optocoupler:

$$V_{IN}=\frac{V_E}{\cos(\pi\times f\times t_{TOTAL})}.$$

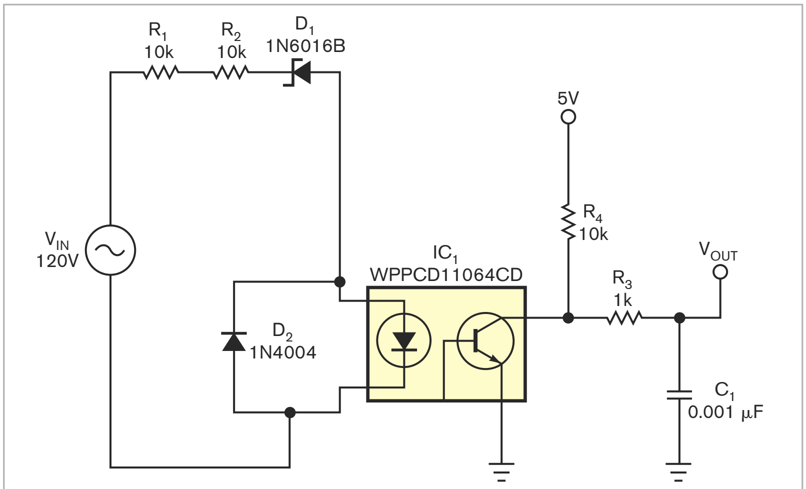

Figure 1 This simple ac-mains voltage monitor's output is a square wave whose width is proportional to the input-voltage level.

You can implement this formula in software or a look-up table that converts pulse width to input voltage. Take note that the input voltage is the peak ac voltage, so you must convert it to the rms value if necessary. You can also use this circuit as a clock line because the output frequency is independent of the duty cycle. The output is consistently 60 Hz, and you can use it for timekeeping. You can also potentially use it for zero-crossing-load driving if you extrapolate the time back to the zero crossing based on the input voltage, because the duty-cycle edge timeshifts from the real zero crossing.

Some other design principles in this circuit require attention. D_2 protects the diode in the optocoupler when the ac input goes negative. In most cases, the optocoupler diode is unaffected because the reverse leakage through the network ensures that the LED does not exceed its maximum reverse voltage. However, bypassing the diode is the best approach for clamping the voltage across this optocoupler using a diode. Adding this diode does more than double the quiescent current in the circuit, and, because you apply this current to the ac line, it may be a concern for both energy consumption and power dissipation in the resistors in the input circuit.

If you need a more accurate estimation of input voltage, some options improve circuit function. The main source of this variation is the 5% tolerance on the zener voltage. A 5% variation on this voltage can result in a significant error in your estimate of the input-voltage amplitude. Specifying a more precise diode or calibrating each board by applying a known input voltage and storing that value in memory as a fixed calibration improve the overall accuracy of this circuit. **EDN**

I^2C interface has galvanic isolation, wired-OR capability, improved noise margin

Michele Costantino, Microsaic Systems Ltd, Woking, United Kingdom

This Design Idea describes a simple and effective way to provide optoisolation for devices connected on the I^2C bus (**Figure 1**). It improves on an earlier version (**Reference 1**). SDA and SCL are on the bus master's side of the I^2C bus; SDA_1 and SCL_1 are on the slave device's side. It is fairly easy to optoisolate the clock line because it is unidirectional, from the master to the slave device. A P-channel MOSFET, Q_3, provides the current for the LED of the fast optocoupler, IC_2, buffering the clock line.

The data line, however, is bidirectional. This section of the circuit is symmetrical. Resistors R_6 and R_7 are the I^2C pullup resistors on the slave device's side of the bus, and R_3 and R_1 are dummy pullups in parallel with the main I^2C pullup resistors on the SDA/SCL side. If both SDA and SDA_1 lines are high—that is, no I^2C devices are pulling them down—Q_1 is off, no current flows into the LED of optocoupler IC_2, IC_2's Pin 7 is high, Q_2 is off, and the LED of optocoupler IC_1 is also off.

THE LED OF IC_1 DOES NOT TURN ON BECAUSE THE VOLTAGE APPLIED ACROSS IT IS BELOW ITS THRESHOLD.

If a device drives the SDA line low, Q_1 and the LED of IC_2 turn off, driving IC_2's Pin 7 low; diode D_2 then starts to conduct. The result is a low level on the SDA_1 line—the low output voltage of IC_2 plus the threshold voltage of Schottky barrier diode D_2. In this situation, it is important to notice that the LED of IC_1 does not turn on because the voltage applied across it is below its threshold. This situation means that the circuit does not latch, and it can recover from this state once you release the SDA line.

Q_3 and the PNP BJT (bipolar-junction transistor), Q_1, effectively buffer the two SDA/SCL lines so that no extra current flows into the open-collector and -drain stages of the I^2C

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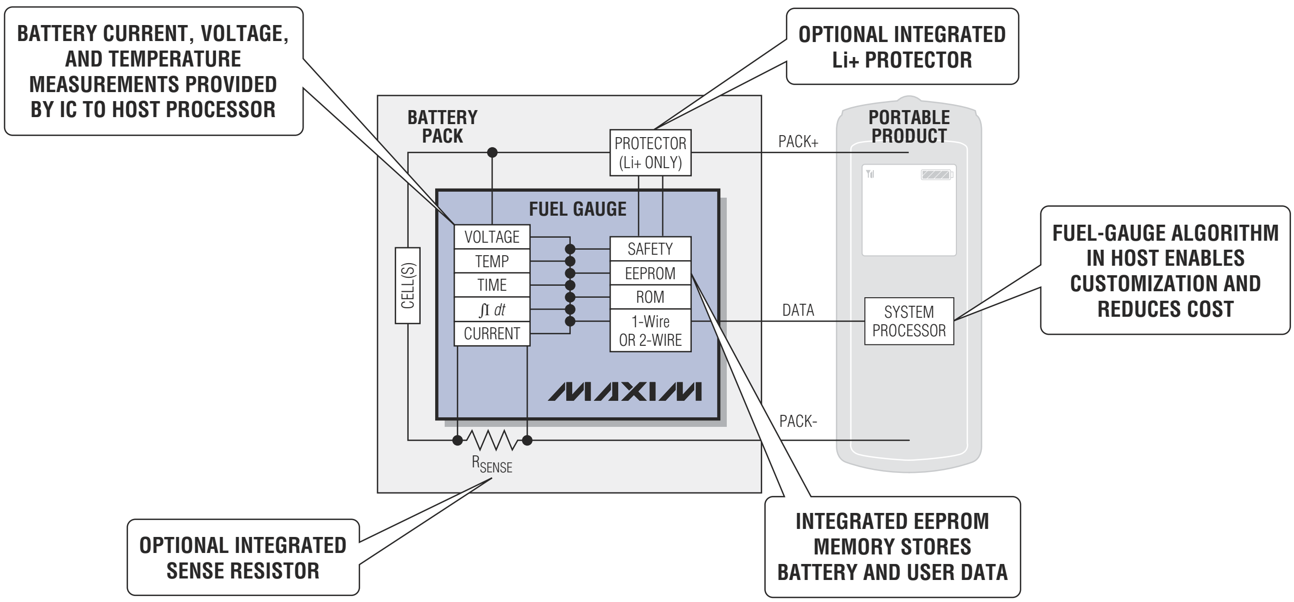

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DS2756	1-Wire	13/16	96	10/11	—	8-TSSOP (3 x 6.4)
DS2762	1-Wire	13	32	10/11	Yes	16-TSSOP (5 x 6.4), flip chip
DS2764	2-wire	13	32	10/11	Yes	16-TSSOP (5 x 6.4)

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devices that connect to the bus when they hold the lines down. This configuration allows the optoisolated interface to repeatedly pull low, providing wired-OR capability. Using Schottky barrier diodes for D_1 and D_2 rather than common diodes reduces the low-level voltage on the bus, improving the noise margin. Finally, because of the low propagation-delay times of the Fairchild Semiconductor (www.fairchildsemi.com) HCPL06XX devices that this design uses, this interface has no bus-glitch problems and works well at speeds of 400 kHz or higher (**Reference 2**).**EDN**

REFERENCES

1. Nguyen, Minh-Tam, and Martin Baumbach, "Two-wire interface has galvanic isolation," *EDN*, Nov 11, 1999, pg 174, www.edn.com/article/CA46286.
2. Blozis, Steve, "Opto-electrical isolation of the I²C-Bus," *Embedded Systems Design*, Oct 14, 2004, www.embedded.com/showArticle.jhtml?articleID=49901764.

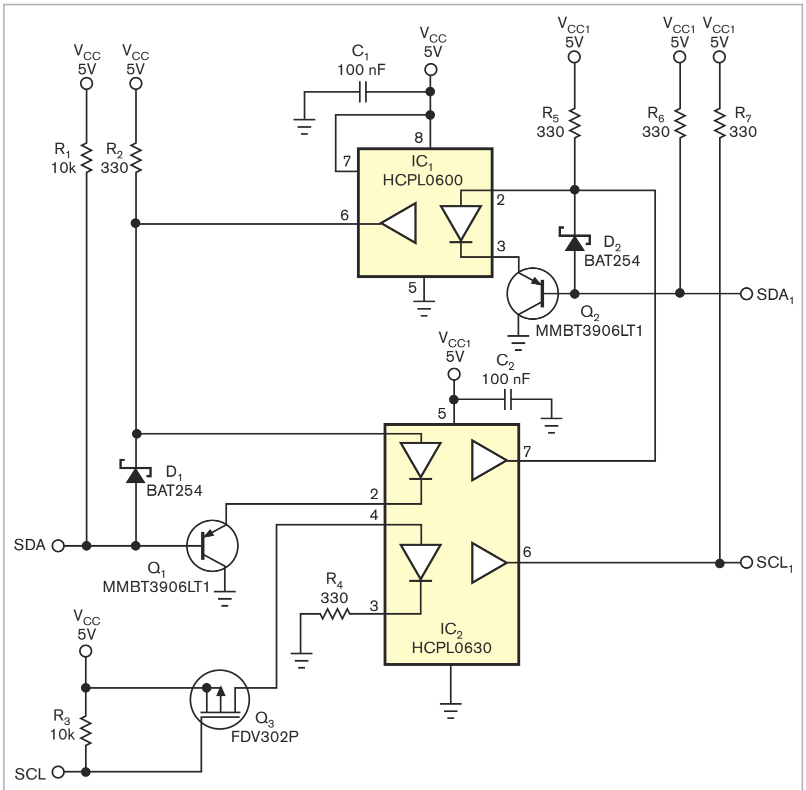

Figure 1 This circuit provides an isolated, bidirectional, wired-OR connection of slave devices to the I²C-bus master.

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DAC122S085	12-bit	2	6 µsec	MSOP-10, LLP-10
DAC084S085	8-bit	4	3 µsec	MSOP-10, LLP-10
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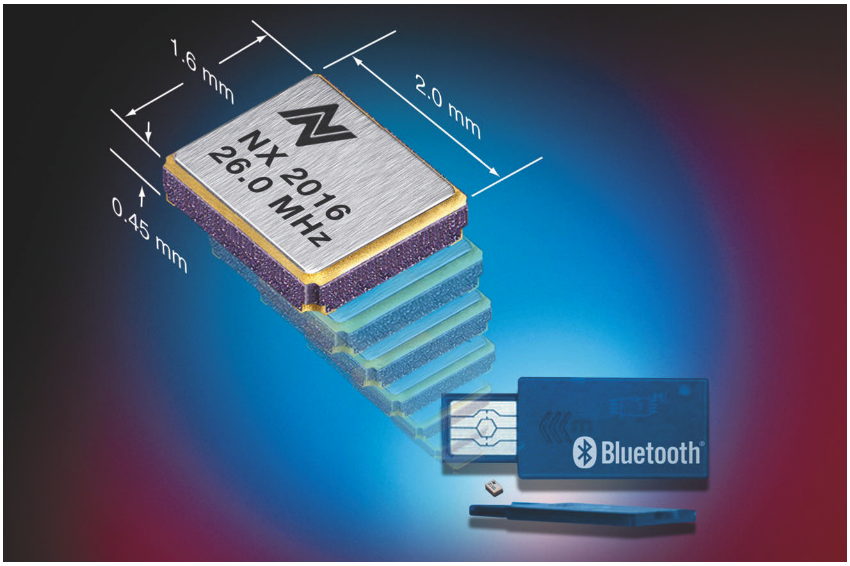


Miniature surface-mount crystals target Bluetooth and ZigBee applications

Operating over a 24- to 80-MHz frequency range and weighing 6 mg, the NX 2016AA thin surface-mount-crystal series suits use in Bluetooth, ZigBee, WLAN, mobile phones, and NFC (near-field communication). The maximum series ESR (equivalent-series resistance) is 100Ω in the 24- to 25-MHz frequency range, 80Ω in the 25- to 36-MHz range, and 60Ω in the 30- to 80-MHz range. Features include a 50-µW drive level, an 8-pF standard load capacitance, and a ±15 to ±100-ppm frequency tolerance over a −10 to +75°C temperature range. Standard frequencies include 24, 26, 27, 28.63636, 32, and 40 MHz. Measuring 2×1.6×0.45 mm, the NX 2016AA costs $1 (10,000).

Nihon Dempa Kogyo, www.ndk.com

MLCCs feature surface arcover prevention

Designed to prevent surface arcover, the VJ HVArc Guard surface-mount X7R MLCC (multilayer-ceramic-chip capacitor) features a 250 to 1000V-dc voltage and a 100-pF to 0.27-µF capacitance. The devices provide maximum capacitance in high-voltage ratings and an increased voltage breakdown. The MLCCs target applications including buck-boost dc/dc converters, voltage multipliers for flyback converters, and lighting-ballast circuits. The VJ HVArc Guard costs 14 cents.

Vishay Intertechnology, www.vishay.com

Surface-mount power inductors have low profiles

Available in four low-profile packages, the HM62 surface-mount power-inductor series provides self-resonant frequencies as high as Q value. The 1-mm-high HM62-2610 inductor features 1- to 22-µH-inductance values at 100 kHz, 0.1V rms, and 0A; it has a ±20 and ±30% absolute tolerance, depending on inductance values. The 1.4-mm-high HM62-3014 has 1- to 100-µH inductance at 100 kHz, 0.1V rms, and 0A; it has a ±20% absolute tolerance. The 1.5-mm-high HM62-3015 has 1.5- to 47-µH inductance at 100 kHz, 0.1V rms, and 0A; it has a ±20 and ±30% absolute tolerance, depending on inductance values. The 1.5-mm-high HM62-3515 has 2.2- to 202-µH inductance at 100 kHz, 0.1V rms, and 0A; it has a ±20% absolute tolerance. Running at a −40 to +85°C temperature range, the HM62 series costs 25 to 35 cents.

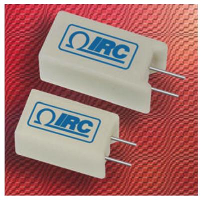
BI Technologies, www.bitechnologies.com

Integrated supercapacitor-charger IC reduces charge time

Targeting high-side-load-switching applications in PC-modem cards, the P-channel AAT4620 current-limited MOSFET power switch charges a supercapacitor, which typically averages out high-pulse currents without exceeding the host-power-supply specifications. This supercapacitor-charger IC integrates circuitry for limiting current, protecting the PC-card connector, continuously charging the capacitor, and notifying the system when it is ready for use. The switch provides two independent programmable-current limits for controlling current during host/card negotiation. When the thermal dissipation is low, the integrated current limiting allows the capacitor to charge to 98% of its final value. Additional features include a 40-µA typicial quiescent current and a 1-µA supply current in shutdown mode. The AAT4620 costs $1.34 (1000).

Advanced Analogic Technologies, www.analogictech.com

Vertical-mount power resistors come in wire-wound and film options



Suiting use in harsh environments, the flameproof, commercial-grade, cement-housed CVW wirewound and CVF film power-resistor series has a vertical-mount configuration for a reduced footprint. The wirewound resistors feature a 0.1 to 910Ω resistance range, and the film resistors have a 28Ω to 200 kΩ resistance range. The devices have ±5 and ±10% standard tolerances, ±400 ppm/°C TCRs (temperature coefficients of resistance) at less than 20Ω, ±350 ppm/°C TCRs at more than 20Ω, and a −55 to +275°C temperature range. Depending on resistance values, the CVW and CVF series resistors sell for 8.5 to 17 cents (10,000).

IRC, www.irctt.com

COMPUTERS AND PERIPHERALS

Entry-level and midrange GPUs provide DirectX 10 gaming

Using 65-nm-process technology, the ATI Radeon HD 2000 midrange and entry-level GPU (graphics-processing-unit) series features. DirectX 10 gaming. The devices feature second-genreation unified-shader architecture. The 2600 and 2400 series feature unified-video-decoder technology, providing high-fidelity, high-definition multimedia playback. The 2900 XT features a 512-Mbyte memory bus, providing full-performance high-dynamic-range rendering. The ATI Radeon HD 2900 XT costs $399, including *Team Fortress 2*, *Portal*, and *Half-Life 2: Episode Two*.

AMD, www.amd.com

Storage processors feature eSATA Gen2m and USB 2.0 host interfaces

Requiring no software, drivers, or special user knowledge, the second-generation Steelvine storage processors feature drive cascading for hot-plug capacity expansion. The SiL5723 suits consumer-electronics devices, DVRs (digital-video recorders), and PC motherboards, featuring a 3-Gbps SATA host interface and two Gen2m eSATA-capable device ports. The Sil5734 combines eSATA and USB 2.0 host interfaces, suiting single-drive external enclosures and external backup drives. The device includes two eSATA ports, an eSATA host port, and a USB 2.0 host port. Aiming at digital-home and small-office storage appliances, the Sil5744 features RAID (redundant array of inexpensive disks) 0 and RAID 1; Safe33 and Safe50 multi-RAID modes; drive locking; and single-button backup. The device also connects a USB 2.0 or an eSATA host port to two eSATA device ports. The Sil5733 has a 3-Gbps SATA host interface and two eSATA-capable device ports. Content security using automatic drive locking allows the device to automatically lock the drive to the host. The second-generation Steelvine storage processors cost $5.

Silicon Image, www.siliconimage.com

GXM device connects three digital monitors to one desktop

The TripleHead2Go digital edition GXM (graphics-expansion module) provides digital-output support for three desktop screens at 3840×1024-pixel resolution. Connecting the dual-

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COMPUTERS AND PERIPHERALS

link DVI (digital-visual-interface) output of a compatible notebook, desktop, or workstation to three digital monitors, the device has a monitor-bezel-management feature that hides part of the image behind the bezel of the monitor. Supporting more than 150 games, the TripleHead2Go digital edition costs $329. **Matrox Graphics, www.matrox.com/graphics**

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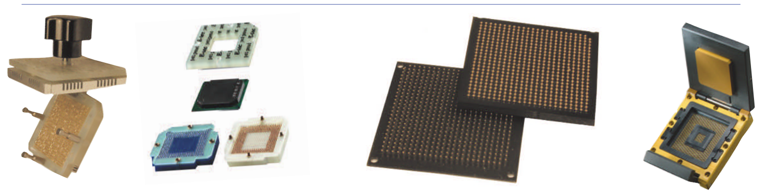

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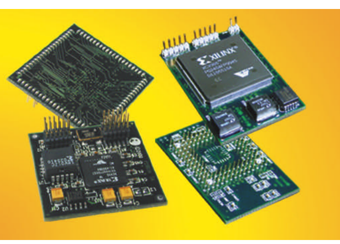

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LOOKING AHEAD

TO SIGGRAPH

What better place to spend those hot August nights than in breezy San Diego—especially if you are involved in computer graphics? SIGGraph (Special Interest Group for Computer Graphics), the Association for Computing Machinery's giant annual event, kicks off August 6 at the waterfront convention center. And center stage will be the big draws for the event: the juried art gallery and the computer-animation festival. Oh, yes. Papers. The 26 paper sessions will cover everything from 3-D-image capture to video processing to the fine points of animation and lighting. It's a world-class event for technical content as well as for shows of art and animation.

LOOKING BACK

AT A CAMERA PHONE, CIRCA 1957

A portable radio facsimile system requires only three minutes to transmit pictures to a companion receiver up to 40 miles away. The set can also send photos over standard telephone lines or via long-range radio circuits. Mounted next to a Jeep radio, the unit transmits a photo suitable for reproduction. A Polaroid camera prepares a picture for the facsimile system in one minute. The facsimile unit, designed by the Signal Engineering Laboratory, then scans and transmits the image to a receiving unit. The receiver picks up the image and records it on a sheet of Polaroid film, which the operator then develops. Total time for taking a photo, transmitting it, and reproducing it is five minutes.

—*Electrical Design News*, July 1957

LOOKING AROUND

AT AN INDUSTRY IN NEUTRAL

Attendance at DAC (Design Automation Conference) last month was disappointing. Analysts say that semiconductor inventories continue to be excessive and have once again cut their outlooks for 2007. What's going on here? One explanation lies in end-user demand. When we say that the electronics industry has become consumer-driven, we have to accept the downside: Consumer markets are not only seasonal, but also fickle. Consumers spend when they are feeling good about their prospects and when there are compelling new products to buy. Both of those factors are issues now. With uncertainty in China about the stock market, less than stellar consumer confidence in the United States, and no particularly new and interesting product concepts coming down the pipe—unless you happen to be a disciple of Steve Jobs—the driver of the electronics industry is asleep at the wheel. And that means the numbers are down, even though things may be going quite well in other segments, such as energy, industrial equipment, and weapons. It's not one big, uniform industry any more.

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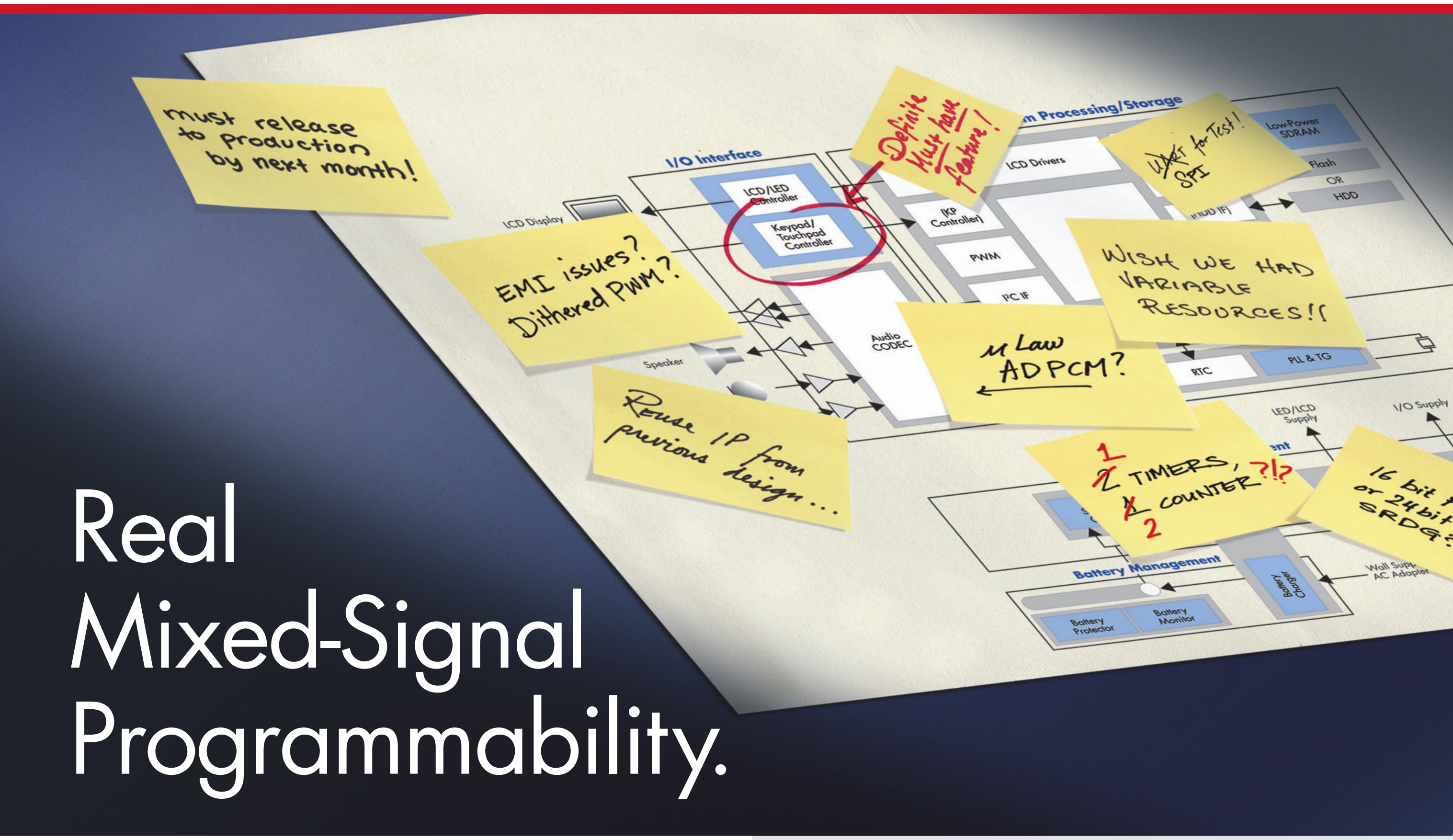

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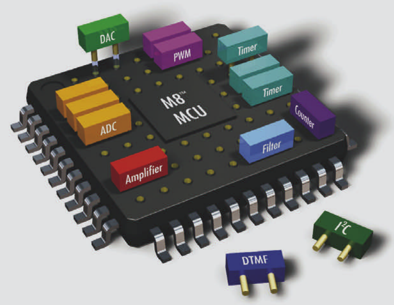

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